CAREER: Energy-Efficient Sensor Networks Using Analog Signal Processing

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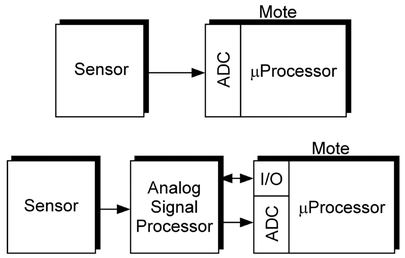
Problem

- Large-scale sensor networks are limited by energy constraints
- Custom analog solutions require extensive design time

Solution

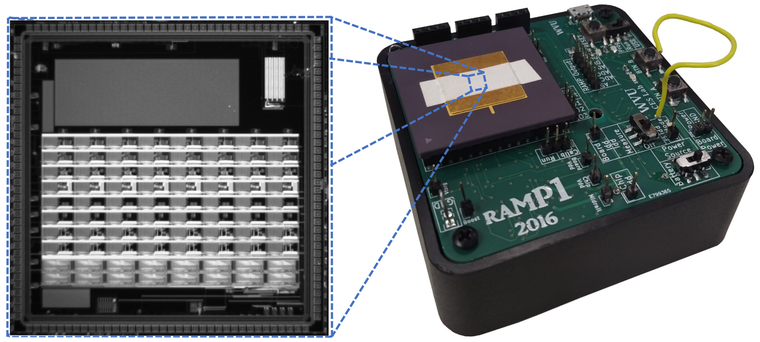
- Provide more local computation at lower power by using analog circuitry
- Provide "reconfigurability" to analog circuits to simplify design of custom applications

Analog Signal Processing (ASP) in Wireless Sensor Networks



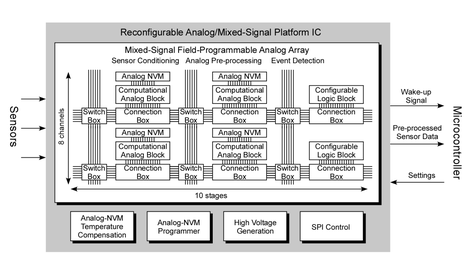
- Conventional systems digitize all sensor information and then process digitally. This wastes power by digitizing / processing unnecessary information
- ASP stage adds signal processing without the need to immediately digitize a signal
- ASP provides signal analysis at ultra-low-power (< 30µW)
- Permits the digital system to hibernate
- Eliminates the use of an MCU for most processing

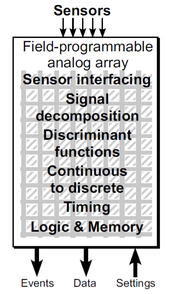
Reconfigurable Analog / Mixed-Signal Processor (RAMP)



- Permits custom, low-power analog designs with minimal effort
- No analog design experience is necessary
- Conceptually similar to a digital field-programmable gate array (FPGA)
- Permits connections between blocks of analog devices
- Integrated-circuit fabricated in a standard CMOS 0.35µm process
- Development board houses MCU, USB, and radio

RAMP Architecture





Computational Elements

- Computational Analog Blocks (CABs)
- Computational Logic Blocks (CLBs)

Configurable Elements

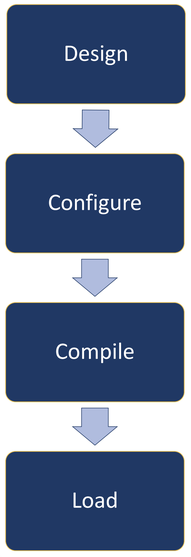
- Analog NVM for tunability and precision
  - 296 analog NVM elements
- SRAM-controlled T-Gates
  - Connection box = Intra-CAB routing
  - Switch box = Inter-CAB routing
  - 20,380 total switches for routing

CAB / CLB Contents

Filtering	Devices
8 BPFs	144 FETs
8 LPFs	8 BJTs
16 Peak detectors	56 Capacitors
Transconductors	16 Resistors
56 OTAs	8 Op-amps
8 Multipliers	Mixed-Signal
8 Correlators	16 S/Hs
References	8 Inverters
48 Prog. current	8 Time-to-voltage
Digital	16 Asym. integ.
16 LUTs	32 Comparators
32 Flip-flops	16 Pulse gen.

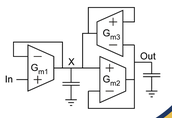
488 Processing Circuits
296 Prog. Parameters

RAMP Synthesis Procedure



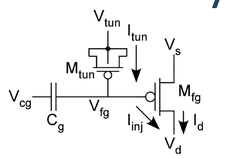
- Utilizes a custom GUI and netlisting scheme for programming the reconfigurable analog system
- **Design:** User creates schematic and netlist. Sets the parameters/coefficients
- **Configure:** Identify primitive blocks from netlist (e.g. bandpass filter)
- **Compile:** Determine routing configuration. Compile routing code. Transform user parameters into circuit biases
- **Load:** Program RAMP via WiFi/MCU

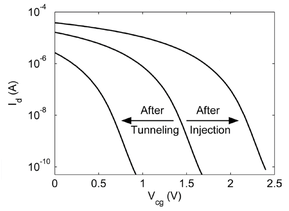
```
begin LPF_Order2 In Out Gm1 Gm2 Gm3
   OTAx Pos=<In> Neg=$X Out=$X Gm-=Gm1
   OTAx Pos=$X Neg=<Out> Out=<Out> Gm-=Gm2
   OTAx Pos=$X Neg=<Out> Out=$X Gm-=Gm3
   Capx Top=$X Bot=Gnd
   Capx Top=<Out> Bot=Gnd
end
```



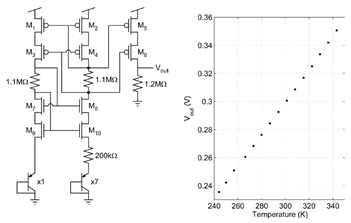
Floating-Gate Nonvolatile Memory

- Core technology used in digital nonvolatile Flash memory, but modified for use as analog nonvolatile memory
- Enabling technology that allows for low-power operation and system reconfiguration in analog systems
- "Tunneling" and "hot-electron injection" modify threshold voltage to desired value
- Precise "programming" of FG charge, used to bias analog circuit elements





RAMP Applications

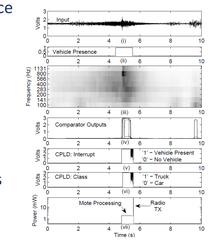


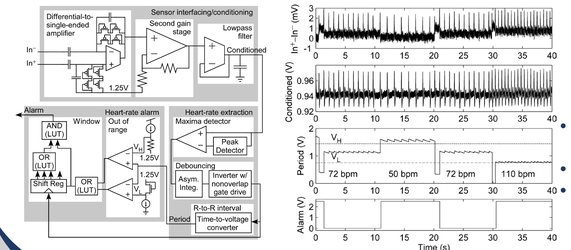
Temperature Sensor

Sensor made from internal RAMP components

Vehicle Detection

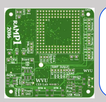
- Determine presence of vehicle using external microphones
- Classify type of vehicle
- All-digital implementation lifetime ~4 months
- Analog version lifetime > 7 years

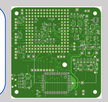




Heart Rate Alarm

- Detects if heart rate is within a healthy range
- Digital solution > 2.3mW
- RAMP solution = 20µW





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