ECGR2181 Logic Design I Spring 2005: Lab 3

Objective
Design a carry lookahead full-adder circuit using Verilog code and load the executable onto the Spartan-3 FPGA board.

General Information
The general steps for this lab are:
1. Write the Verilog code for a 4-bit Carry look ahead Fulladder.   Bring it to the lab session. The adder must be carry look ahead for any credit.
2. Follow the instruction manual to synthesize the Verilog for your designs.
3. Obtain a development board and programming cable.
4. Load the Spartan-3 Board on PCs in Smith 347. Follow the instruction manual to download the full-adder Spartan-3 board.
5. Build the project and load onto your board. Run the program and observe the operation.
6. Demonstrate for a TA.

Laboratory Assignment Requirements
1. **Create a new directory for Lab03. Save the Verilog files as *filename.vl* in the same directory.**
2. The code is well commented and easy to follow.
3. The code (and board) demonstrates the truth tables shown below.
4. The design uses the switch and light assignments defined below.
4. Turn in a lab report with your Verilog code.

Hint: Refer Page 434-435 on your book. Have the given circuit as your reference design.

Test data/process:

Cin	X0	X1	X2	X3	Y0	Y1	Y2	Y3	S0	S1	S2	S3	Carry out
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	1	0	1	1	1	1
0	1	0	0	0	1	0	0	0	0	1	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	1

Lab Report
Use the lab report format provided for the last lab. Write the one page report and include a hard copy of your Verilog code.
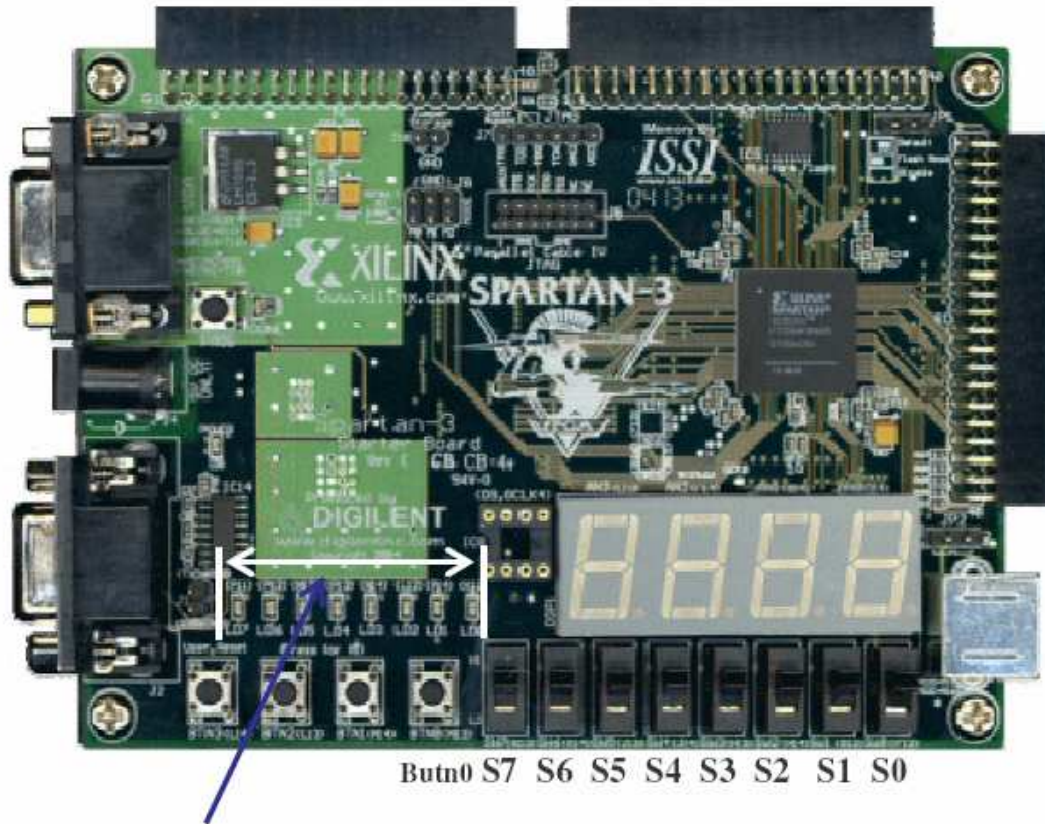
Butn0 S7 S6 S5 S4 S3 S2 S1 S0

L7 L6 L5 L4 L3 L2 L1 L0

Input	x0	–	Switch 0	Port f12
Input	x1	–	Switch 1	Port g12
Input	x2	–	Switch 2	Port h14
Input	x3	–	Switch 3	Port h13
Input	y0	–	Switch 4	Port j14
Input	y1	–	Switch 5	Port j13
Input	y2	–	Switch 6	Port k14
Input	y3	–	Switch 7	Port k13
Input	Carry-In	–	Button 0	Port m13
Output	Sum0	–	LED0	Port k12
Output	Sum1	–	LED1	Port p14
Output	Sum2	–	LED2	Port l12
Output	Sum3	–	LED3	Port n14
Output	Carry	–	LED7	Port p11