Name:	
Date:	

ECGR 2181 - Logic System Design I

Lab 1

1. Draw the truth table for the equation (AB)' + C = Y

2. Describe the circuit using VHDL and simulate it. (Hint: Take the files and projects developed in the lab manual and modify it accordingly to the new equation.

Turn in a copy of your VHDL code file

Turn in a copy of the simulation waveform showing all possible combinations of inputs.