ECGR 2181 - Logic System Design I

INSTRUCTIONS FOR LAB I

Step I

The code required to complete the lab assignment is already provided. A few changes must be made to make the code work for the given Boolean equation. On the computer create a new directory for your project with the following format: ***C:\ECGR_2181 \student_name\lab01.***

1. Download the files ***lab01.vhd*** and ***lab01_tb.vhd*** provided at the lab website and save them in the directory ***C:\ECGR_2181 \student_name\lab01***

2. Start the **Xilinx Project Navigator** from the desktop.

3. Create a new project; In the Project Navigator, select ***File → New Project***. This will bring up a window like the one shown in figure 2. Setup ***lab01*** as the name for your project and then click on the **...** button to browse to your directory. Choose ***HDL*** for ***Top-Level Module Type***; because we will be implementing the project in VHDL, which is a Hardware Descriptive Language (HDL). Once the correct options have been chosen, click ***Next***.

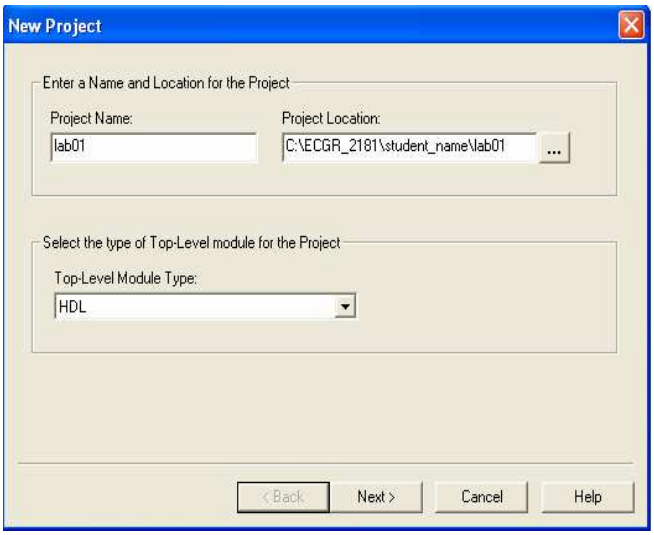


Figure 2. New Project options

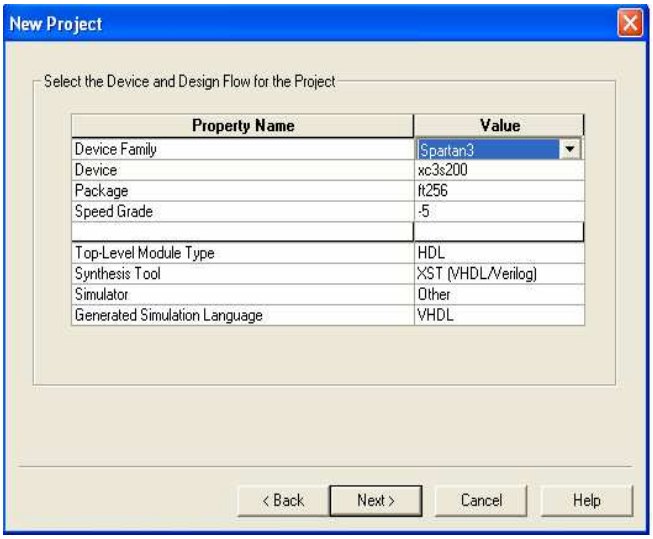


Figure 3. Device Options

4. Setting a device; The next window allows us to choose the type of device we will be using for the project. Since lab01 has only simulation of this project, the device type does not really matter this time. We just need to pick a device that is big enough to store the project. Choose the settings like the ones shown in figure 3, click ***Next***.

5. Adding or creating new source files; The next window allows you to create a new source. We need to add existing sources to the project so click ***Next***. Now we can add our existing sources to the project. Click ***Add Source***. Browse to your directory and choose ***lab01.vhd*** and click ***Open***. In the next window, make sure ***VHDL Design File*** is highlighted (as shown in figure 4), click ***OK***.

Figure 4

Figure 5

6. Now add the ***lab01_tb.vhd*** file to your project, but make sure ***VHDL Test Bench File*** is selected as the source type as shown in figure 5. Now the final window should look like the one shown in figure 6. When you are done adding your files click ***Next***.

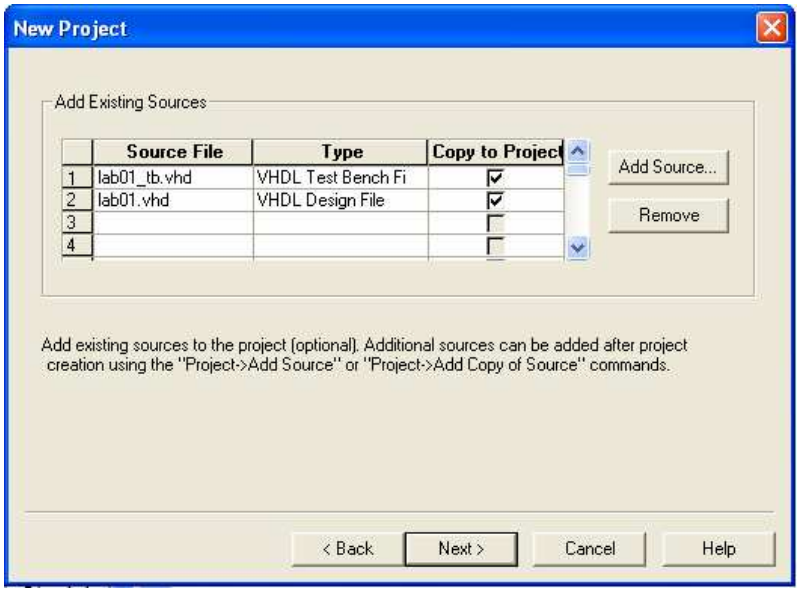
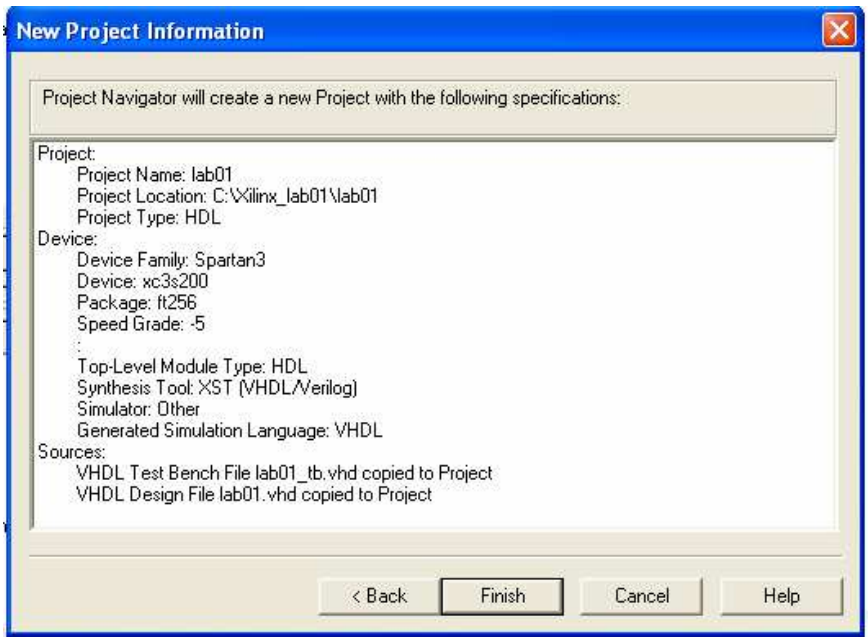


Figure 6. Files added to the project

The next window is a summary of all of the settings of you project. Verify that they are correct and click ***Finish***. Project Navigator is now showing your newly created project. Spend some time analyzing the code. Determine what it is actually doing.



Step II

Analyze and Compile the Code

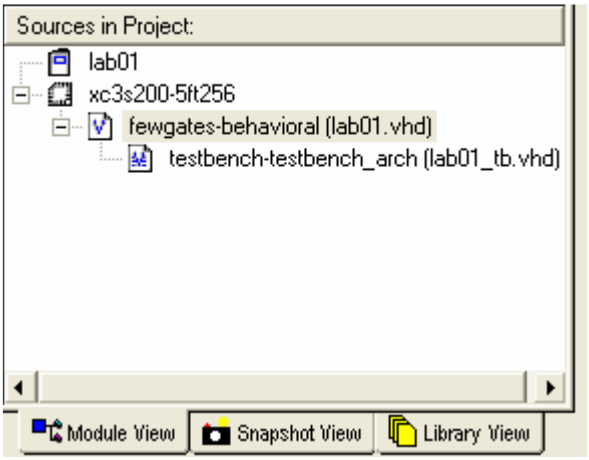


Figure 7

Look for the ***Sources in Project*** box in the upper left corner of the window. Notice how the test bench code falls below the main code, ***lab01.vhd***, in a hierarchical level as shown in figure 7. This is based on the concept that the test bench would serve no purpose without the main code. The test bench serves only to test the main code. Figure 7. Hierarchical level for files Double click on ***fewgates-behavioral (lab01.vhd)***. This will open the file so that it can be edited; note the way the software color-codes the code (green for comments, blue for keyword/reserved words, etc. as shown in figure 8). This feature can be used as an error detection technique. It can sometimes help find code problems. Close the ***lab01.vhd*** code.

```
1  --*********************************************
2  -- File: lab01.vhd
3  --Name:
4  --Date:
5  --Lab Partner:
6  --*********************************************
7  --Defining the library packages to be used
8
9
10 library IEEE;
11 use IEEE.STD_LOGIC_1164.ALL;
12 use IEEE.STD_LOGIC_ARITH.ALL;
13 use IEEE.STD_LOGIC_UNSIGNED.ALL;
14
15 --Declaration of the module's inputs and outputs
16 entity fewgates is port (
17
18 A: in std_logic;
19 B: in std_logic;
20 C: in std_logic;
21 Y: out std_logic
22
23 );
24 end fewgates;
```

Figure 8. Comments and color-codes in a VHDL file.

1. Synthesize the project; Highlight the ***lab01.vhd*** code (in the ***Sources in Project*** box) and then expand the ***Synthesize*** section within the ***Processes for Source*** box and double click ***Check Syntax***. The syntax check should indicate no errors. To see how it looks with errors, change some letters in the ***lab01.vhd*** code and do the process again. A green check mark is conformation that the syntax check was successful as shown in figure 9.

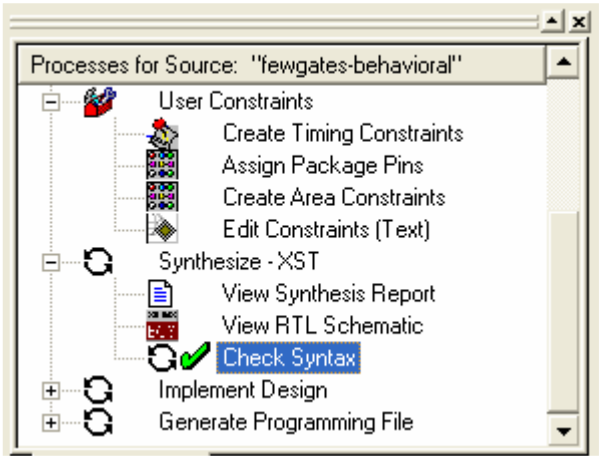


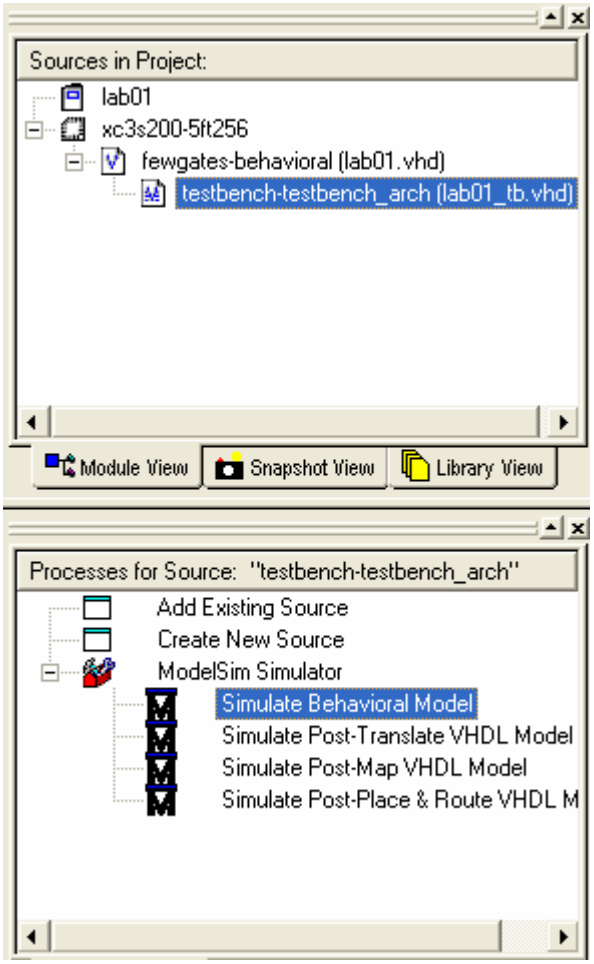
Figure 9. Green check mark showing the process was successful.

Step III

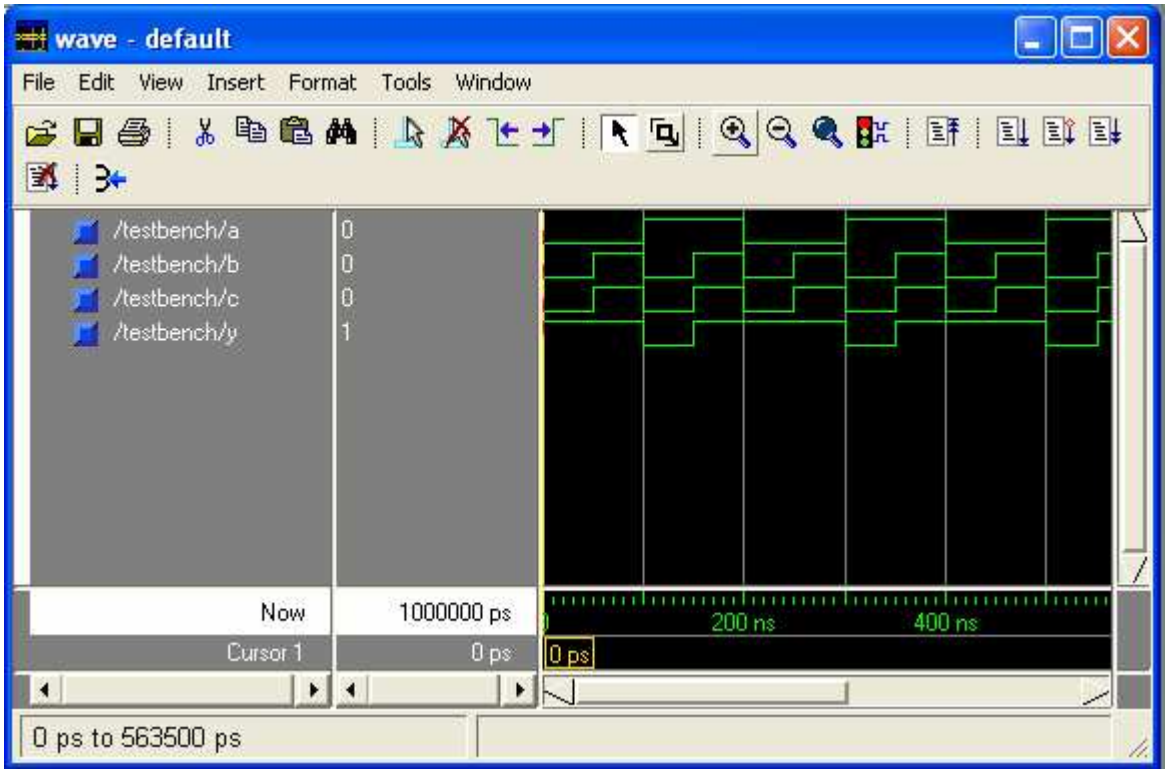
Simulate the system

The next step is to simulate this design. Simulation gives the ability to ensure a project does what is expected

1. Run behavioral simulation; Highlight the file ***lab01_tb.vhd*** in the ***Sources in Project*** window and double click on ***Simulate Behavioral Model*** in the ***Processes for current sources*** window. This tells the Xilinx software to launch ModelSim and use the test bench file to test the main code.



Four new ModelSim windows will appear. For this lab, only the one titled wave - default (a black screen with green lines) will be utilized. Expand the waveform by clicking on the magnifying glass that says Zoom Full. The waveform should look like the following.



Now it can be seen that anytime ***a*** and ***b*** are low or ***c*** is high, ***y*** will be high. This could be thought of in terms of voltages with the lower line being 0 volts and the elevated line being 5 volts. Click anywhere on the waveform. This will create a cursor that can be moved across the waveform. This will show the input and output status at various times.