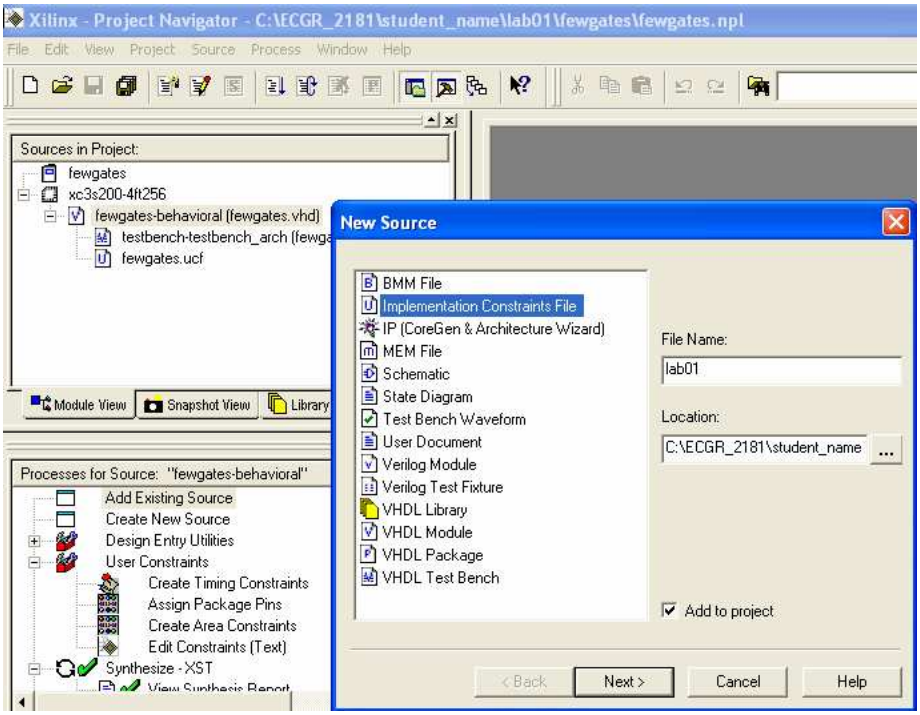
Downloading the code into Spartan-3 Board

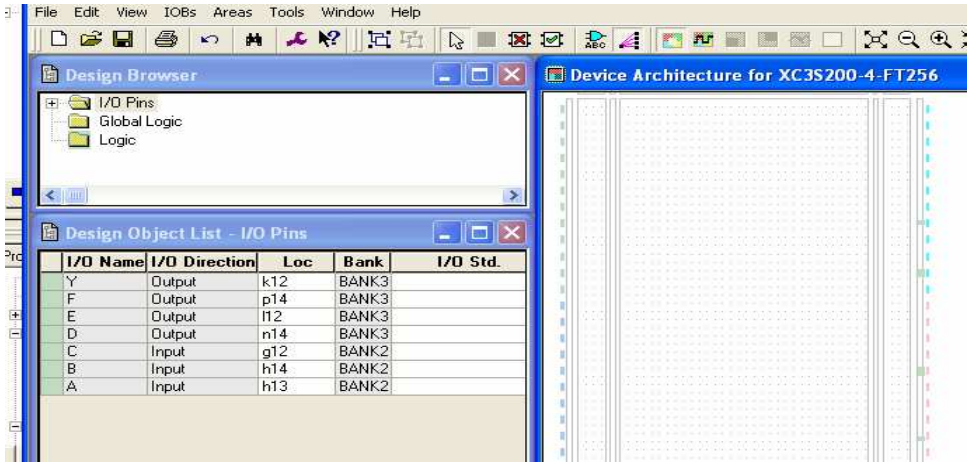
In Order to download the code into the FPGA board we need our simulate file in *.bit* format. The Xilinx software is compatible with Spartan-3 board and has all the necessary features to generate and download the simulated file into the board.

Generating the .BIT file for programming the Digilent S3 Board
Once your design simulates correctly, you can download the design bit-stream onto the Spartan-3 board and test it.

- First you have to provide pin assignments for inputs and outputs. Right click on the file at the highest level of hierarchy in the *Sources in Project* window and go to *New Source*.



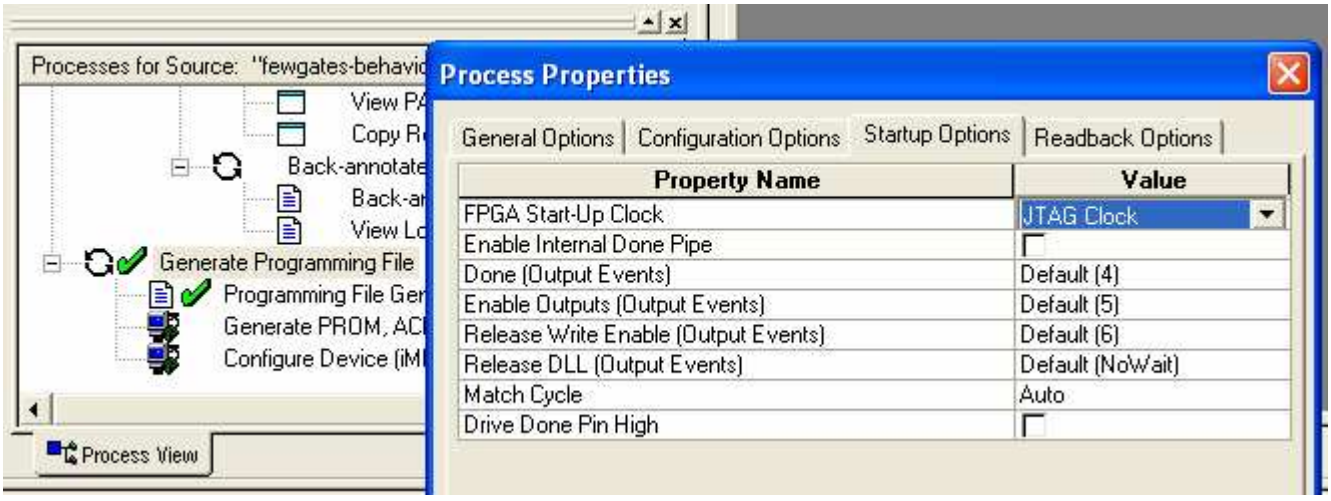
- In the box on the left, select *Implementation Constraints File*. (.ucf)
- Enter the <filename> of you choice. It is recommended that the UCF file has the same name as the top-level entity.
- Click *Next*
- Select the source file which contains the top-level entity. It is the same as the file at the highest level of hierarchy in the *Sources in Project* window.
- Click *Next*à *Finish.*
- The new <filename>.ucf file will appear in the *Sources in Project* window
- Double click on the UCF file to edit it.



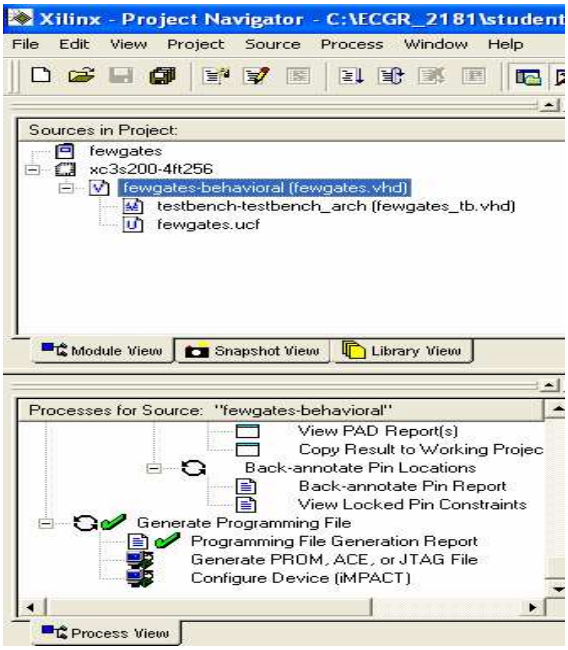
- This will open Xilinx Constraints Editor. Click on the *Ports* tab above the log window. You should see a table with input/output ports listed. In the *Location* column, type in the pin assignments for corresponding input/output ports as provided in the description of the appropriate experiment.
- Make sure you hit ENTER after every change to the *Location* column.

- Once you have entered the pin assignments for all ports, save the file and exit the Constraints Editor. You will be asked to *Run Translate* again, click *OK*. You will be asked to *Reset Implement Design Process*, click *Reset*. Double click on *Implement Design* in the *Processes for Current Source* window to make the pin assignments effective. If asked, choose to reload the files that are modified.

- (NOTE: This step needs to be done only once per project). Select the file at the highest level of hierarchy in the *Sources in Project* window and right-click on the *Generate Programming File* in the *Processes for Current Source* window. Select *Properties*. from the drop-down menu. In the Process Properties dialog box, select the .Startup Options. tab. Change the FPGA Start-Up Clock to JTAG Clock and click the OK button.



• Double-click on *Generate Programming File* in the *Processes for Current Source* window. This will generate a <*projectname*>.*bit* file that will be used to program the FPGA on the Digilent S3 board.

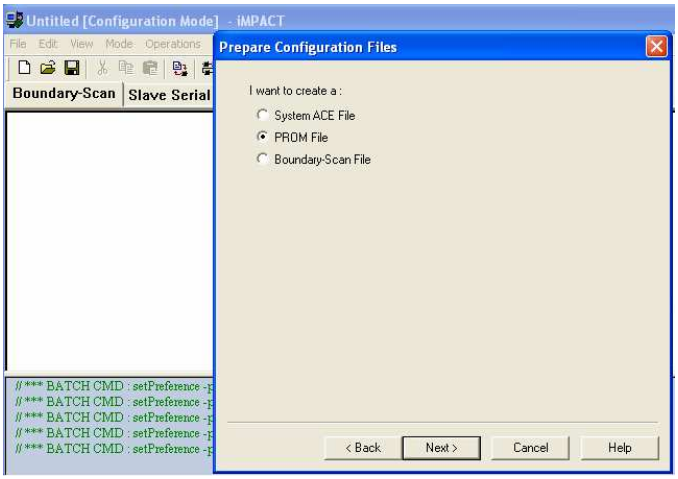


Generating the PROM file for programming the on-board FLASH

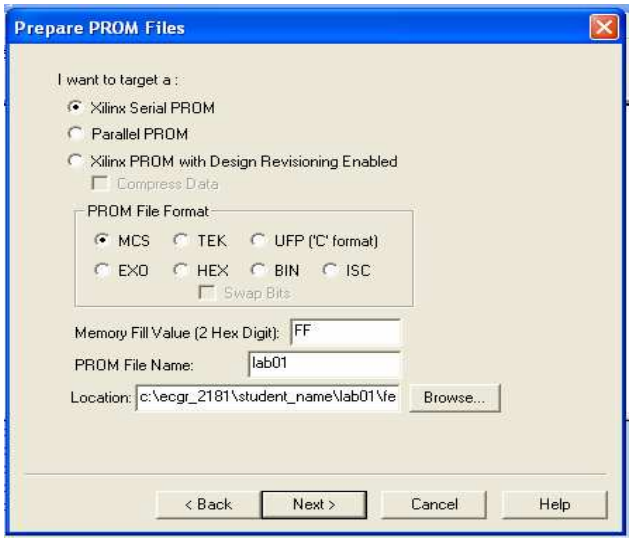
A tool called iMPACT is used to create the file for the on-board PROM flash memory. The PROM will keep a copy of your FPGA design and program the FPGA after a reset.

• Double-click on *Generate PROM, ACE or JTAG File*

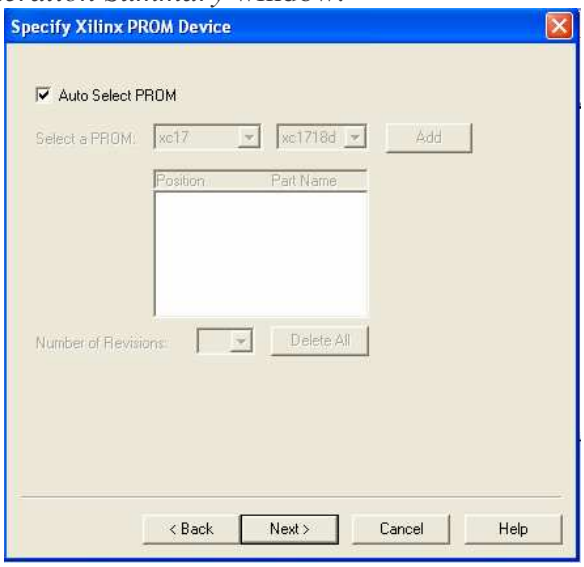
• This will launch the iMPACT software and the *Prepare Configuration Files* window. Select *PROM File* and hit *Next*.



• In the *Prepare PROM File* window, change the name of the PROM file from *Untitled* to the <*lab01*>. Don't change any other option. Hit *Next*.



- Check the *Auto Select PROM Device* in the next window and click *Next.*
- Click *Next* in the *File Generation Summary* window.



- Click the *Add File*. button, select the *<lab01>.bit* file and click *Open.*

• A warning will pop-up:

WARNING:iMPACT:1050 . Startup Clock has been changed to .Cclk. in the bitstream stored in memory, but the original bitstream file remains unchanged.
Ignore this warning. Click OK.

• Click *No* when asked whether *You would like to add another design file to Data Stream: 0?*

• Click *Finish*.
• *Yes*, you want to generate file NOW?
• You will see the Xilinx PROM icon pointing to the xc3s200 <projectname>.bit icon. This means a <*projectname*>*.mcs* has been created in your project directory.
• NOTE: iMPACT might minimize itself after it finishes generating the PROM file. Check your taskbar. It will be there.
• Close iMPACT.

Downloading Design on the Digilent S3 Board
A tool called iMPACT sends the completed bitstream to the FPGA. Like the rest of the tools, it seems to have a few bugs. Take the following steps to program the FPGA with your bitstream:
• Connect the programming cable to the computer.s parallel port and the board.s JTAG connector.
• Power on the dev board.
• Double click on *Configure Device (iMPACT)*
• Select *Boundary Scan Mode* Click *Next*
• Select *Automatically connect to cable*.
• iMPACT will detect 2 devices in the boundary-scan chain. Now you will start selecting the programming files starting with the first.
• Select the <*projectname*>*.bit* file
• For the second file, select <*projectname*>*.mcs* file.
• Right click the first icon. This signifies the FPGA itself. Select *Program*. in the drop down menu, UNCHECK the *Verify* checkbox. Hit OK. Ignore any warnings.

• Right click the second icon. This signifies the PROM on the board. Program the PROM in a similar fashion.
• The FPGA should be programmed and running your design now.