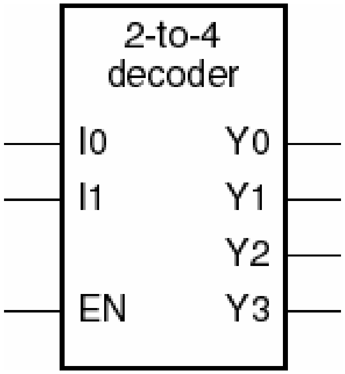
Decoders and Encoders

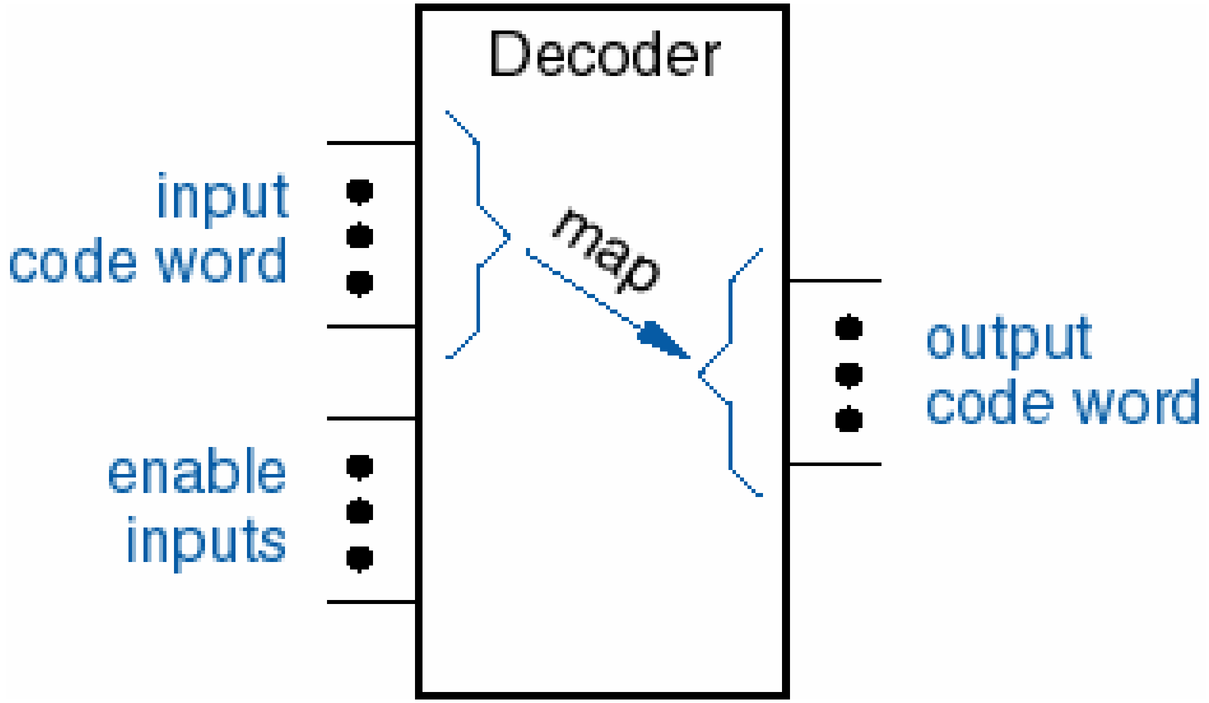
ECGR2181



Reading: Chapter 5.4 and 5.5

Decoders

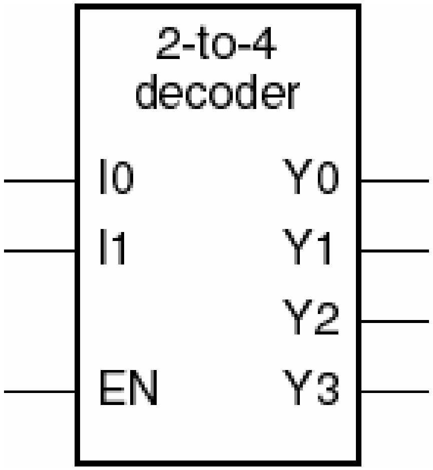
General decoder structure

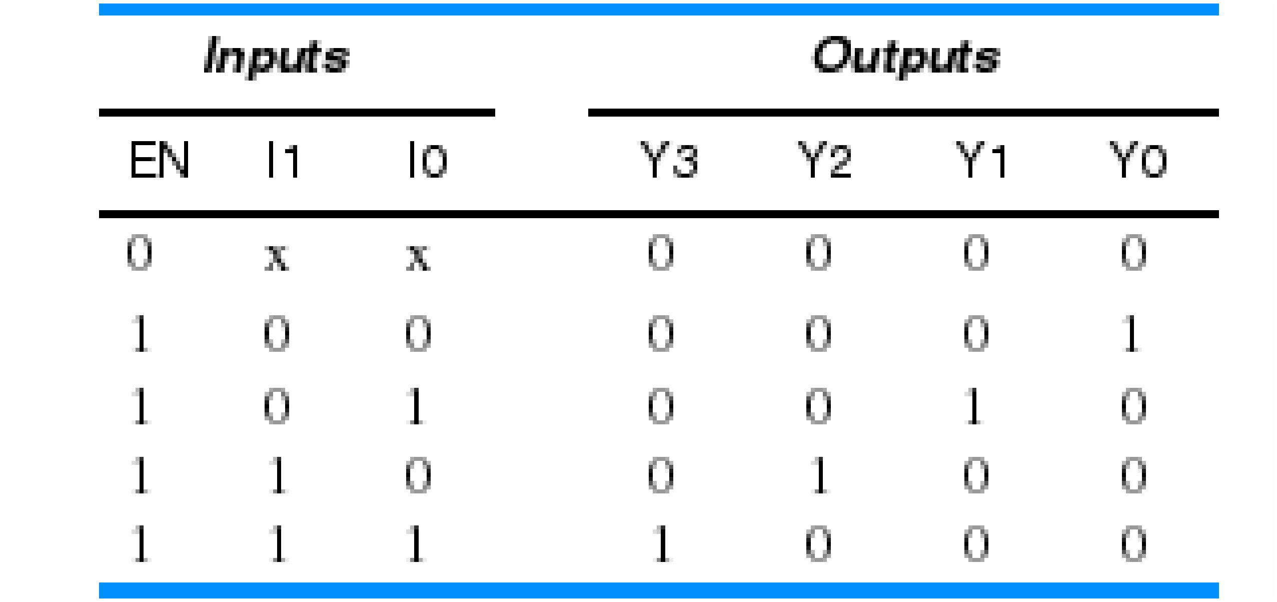


Typically n inputs, 2^n outputs

- 2-to-4, 3-to-8, 4-to-16, etc.

Binary 2-to-4 decoder

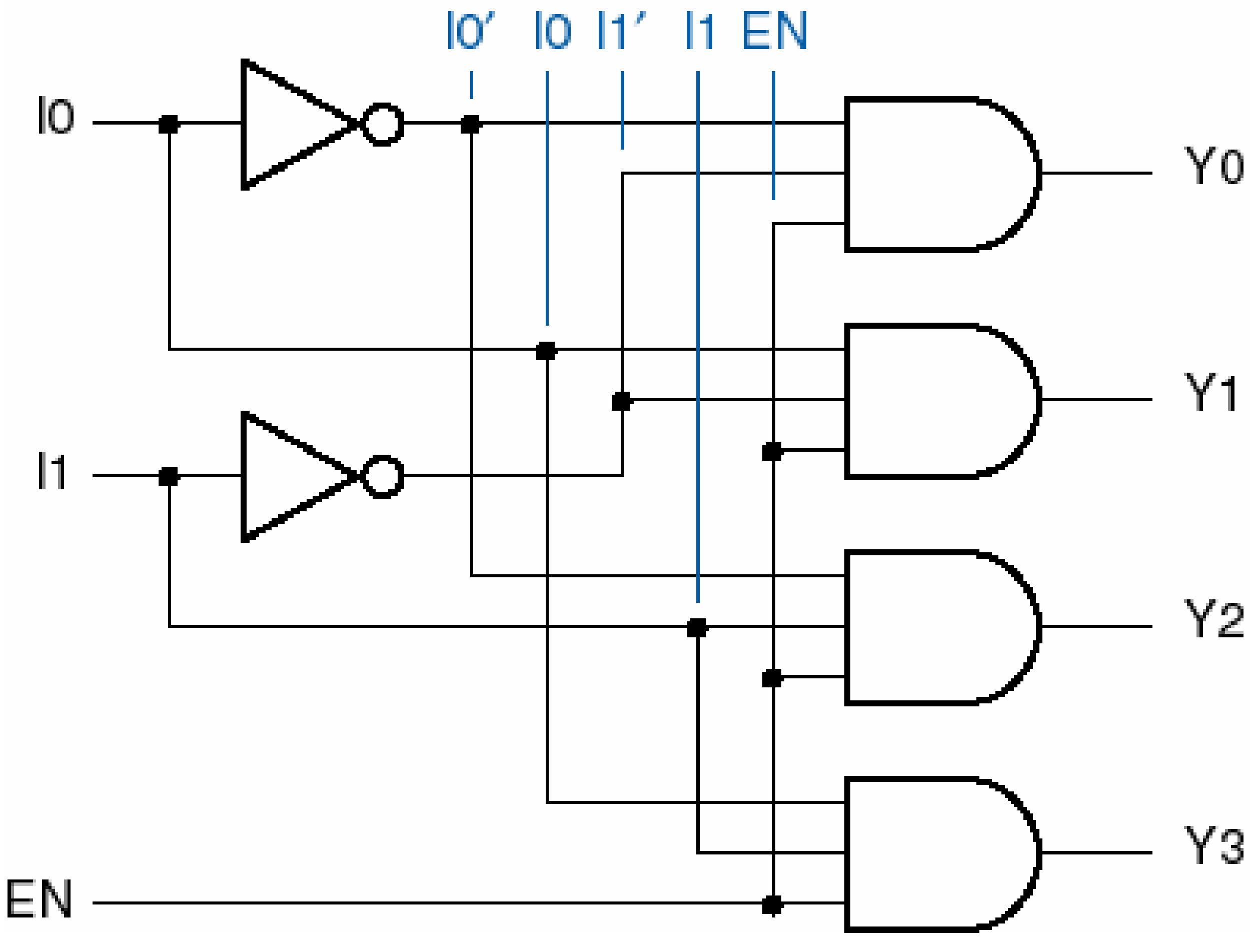




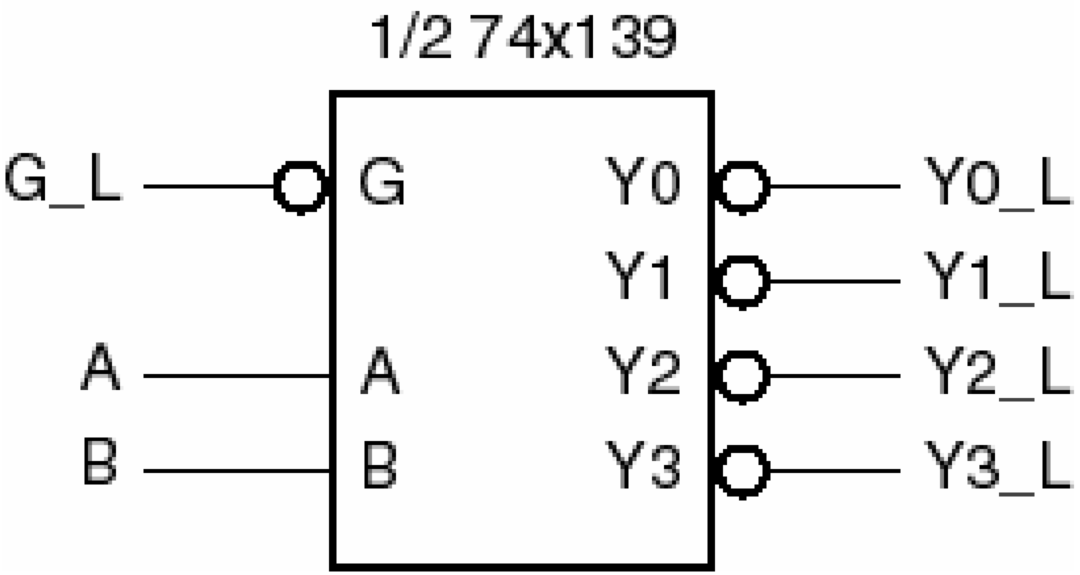
Inputs			Outputs			
EN	I1	I0	Y3	Y2	Y1	Y0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

Note “x” (don’t care) notation.

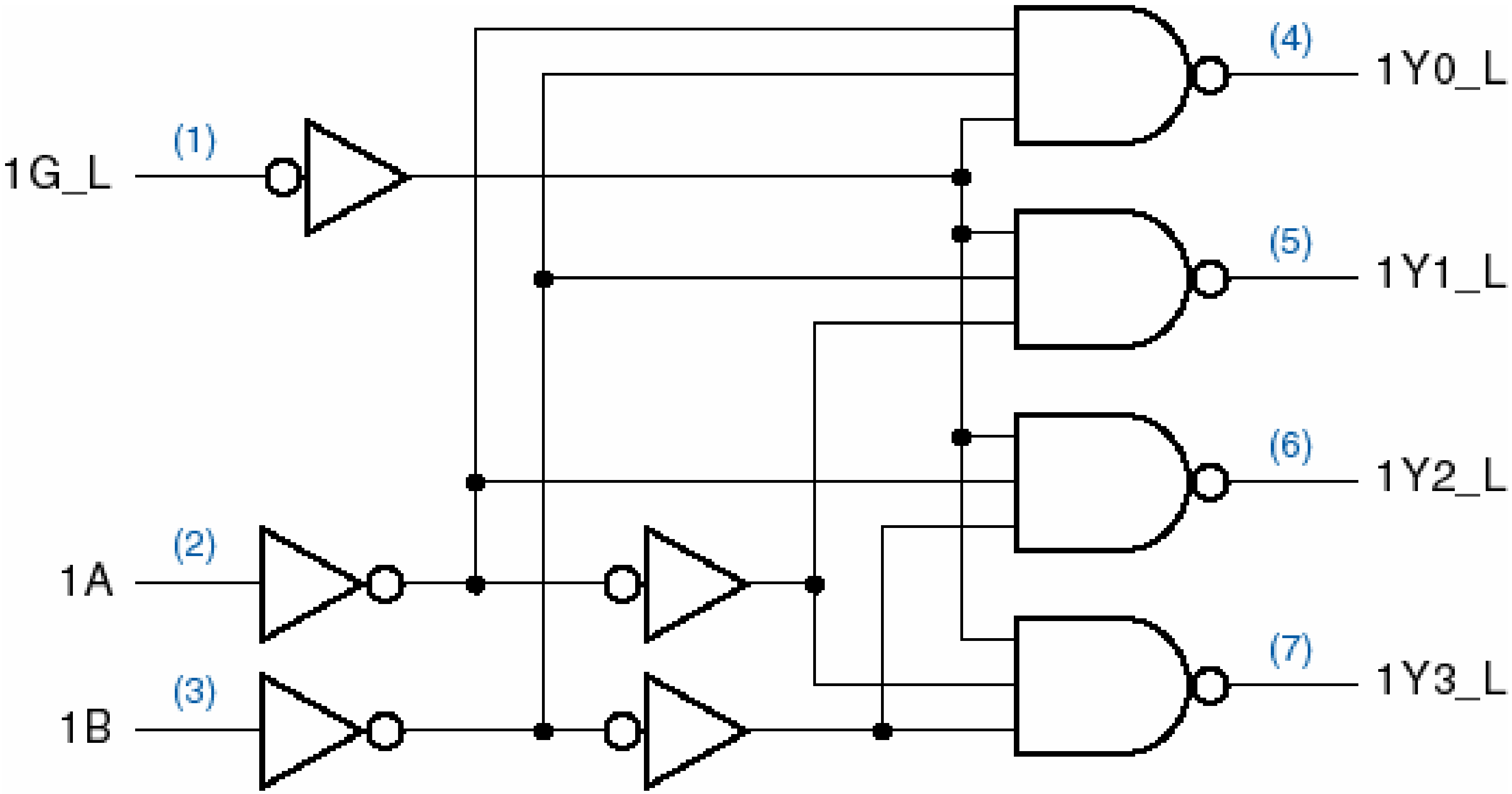
2-to-4-decoder logic diagram



Decoder Symbol



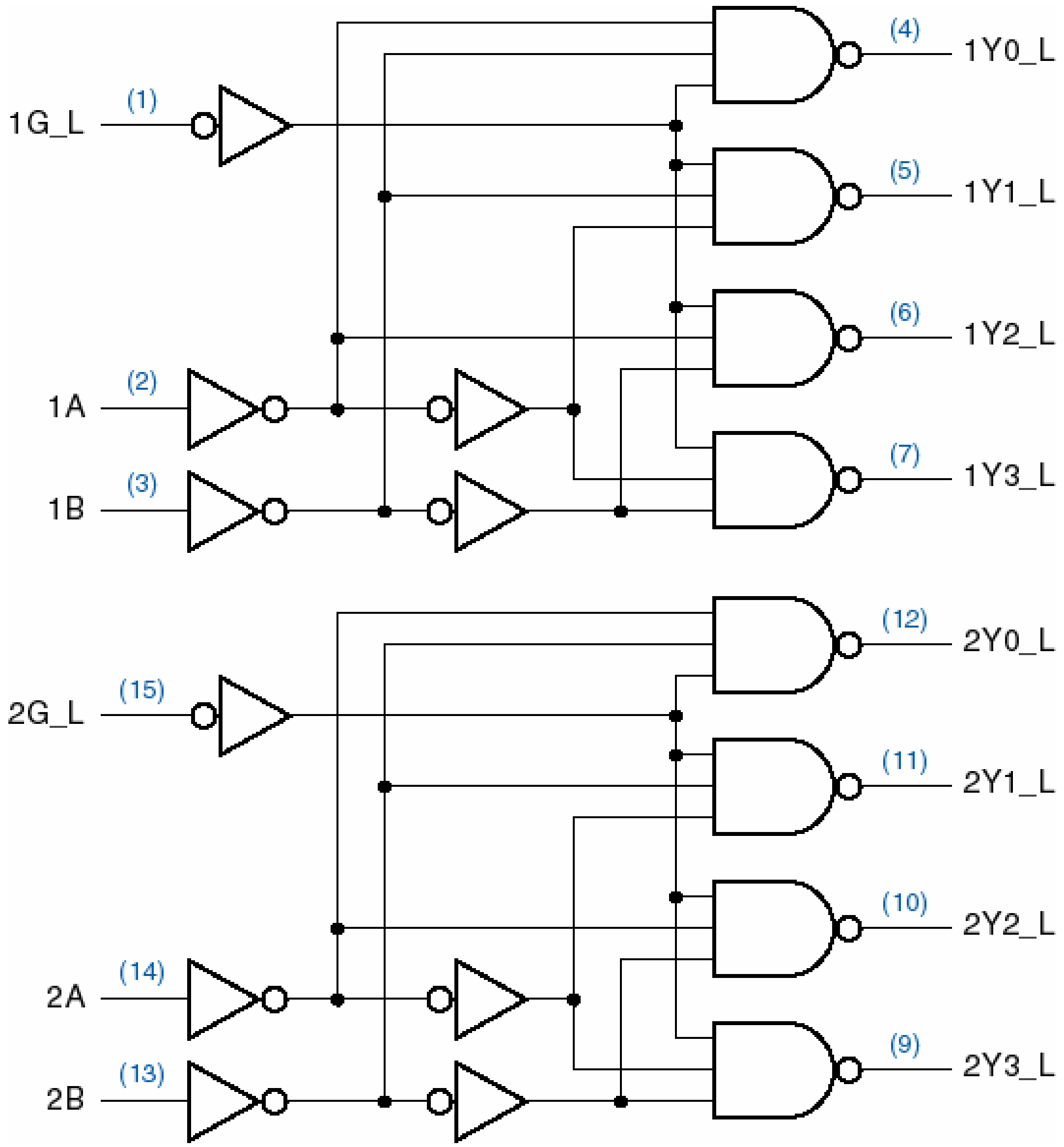
MSI 2-to-4 decoder

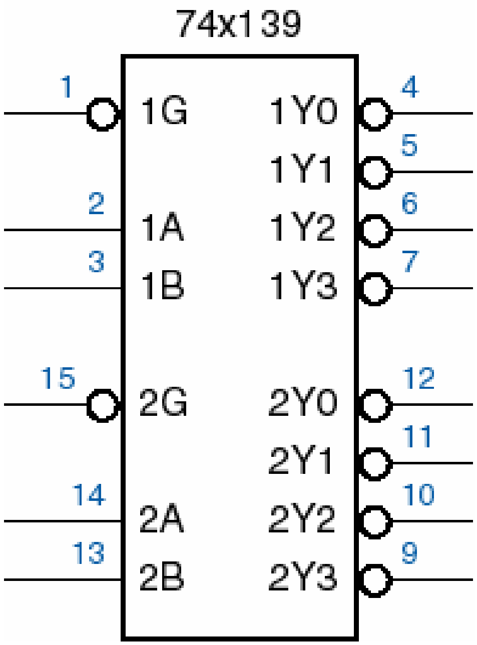


Input buffering (less load)

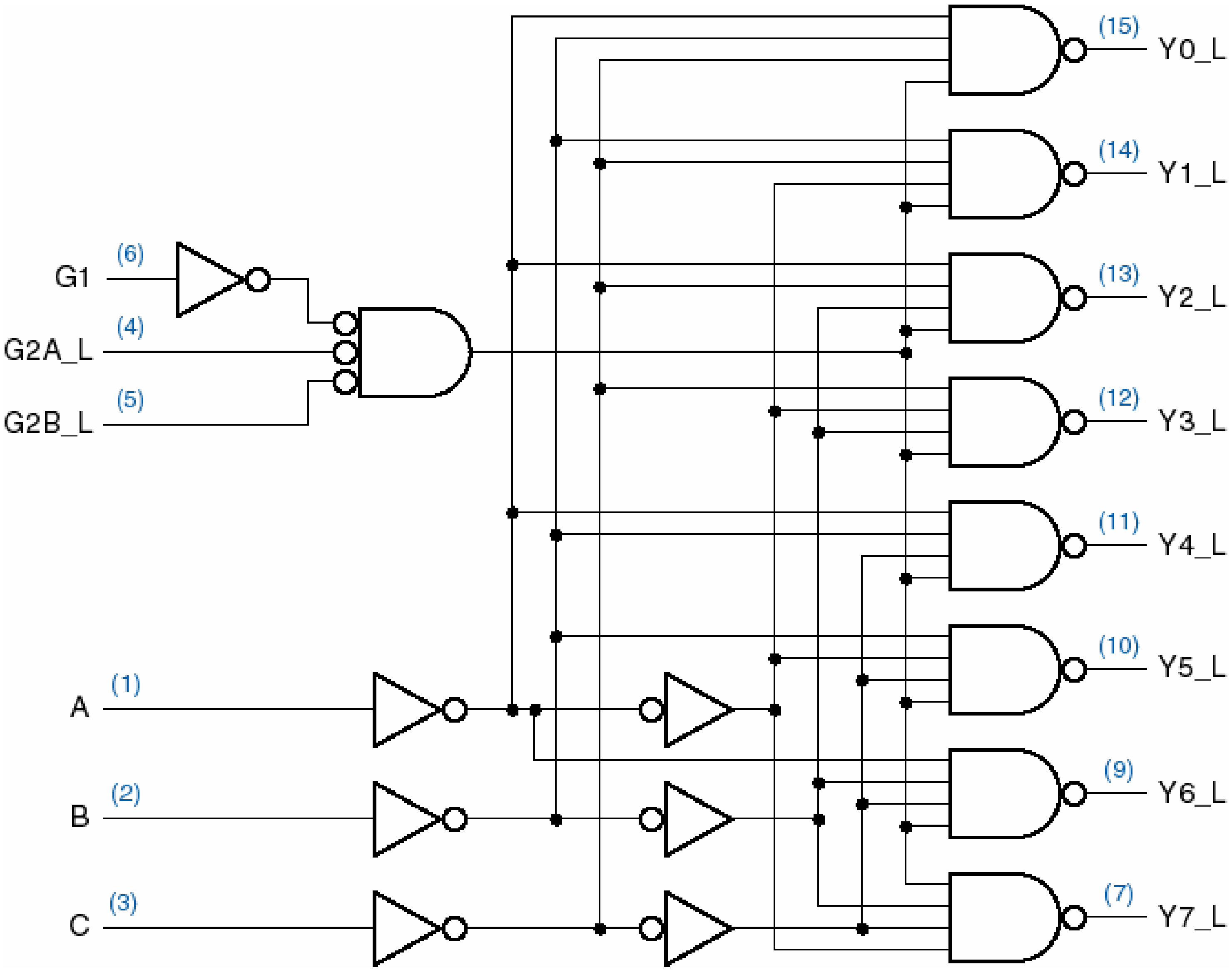
NAND gates (faster)

Complete 74x139 Decoder

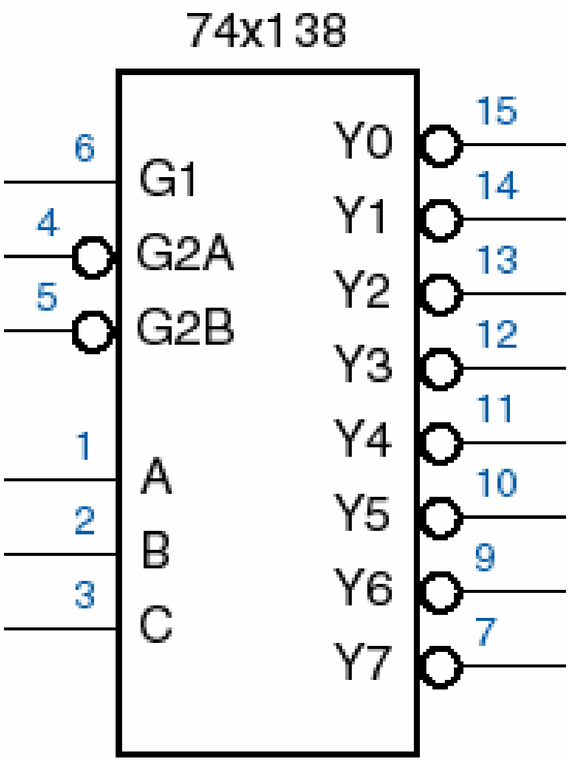




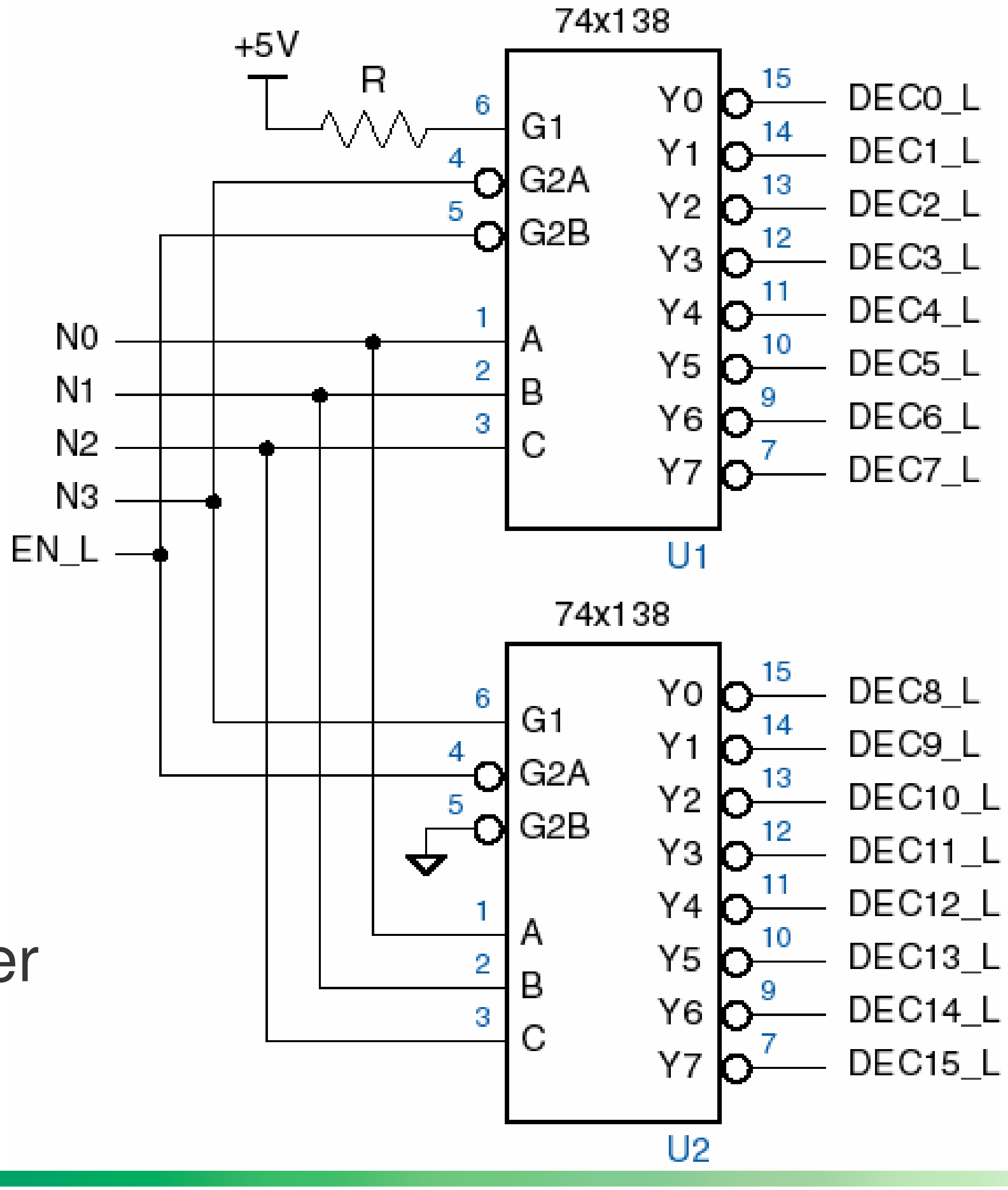
3-to-8 decoder



74x138 3-to-8-decoder symbol

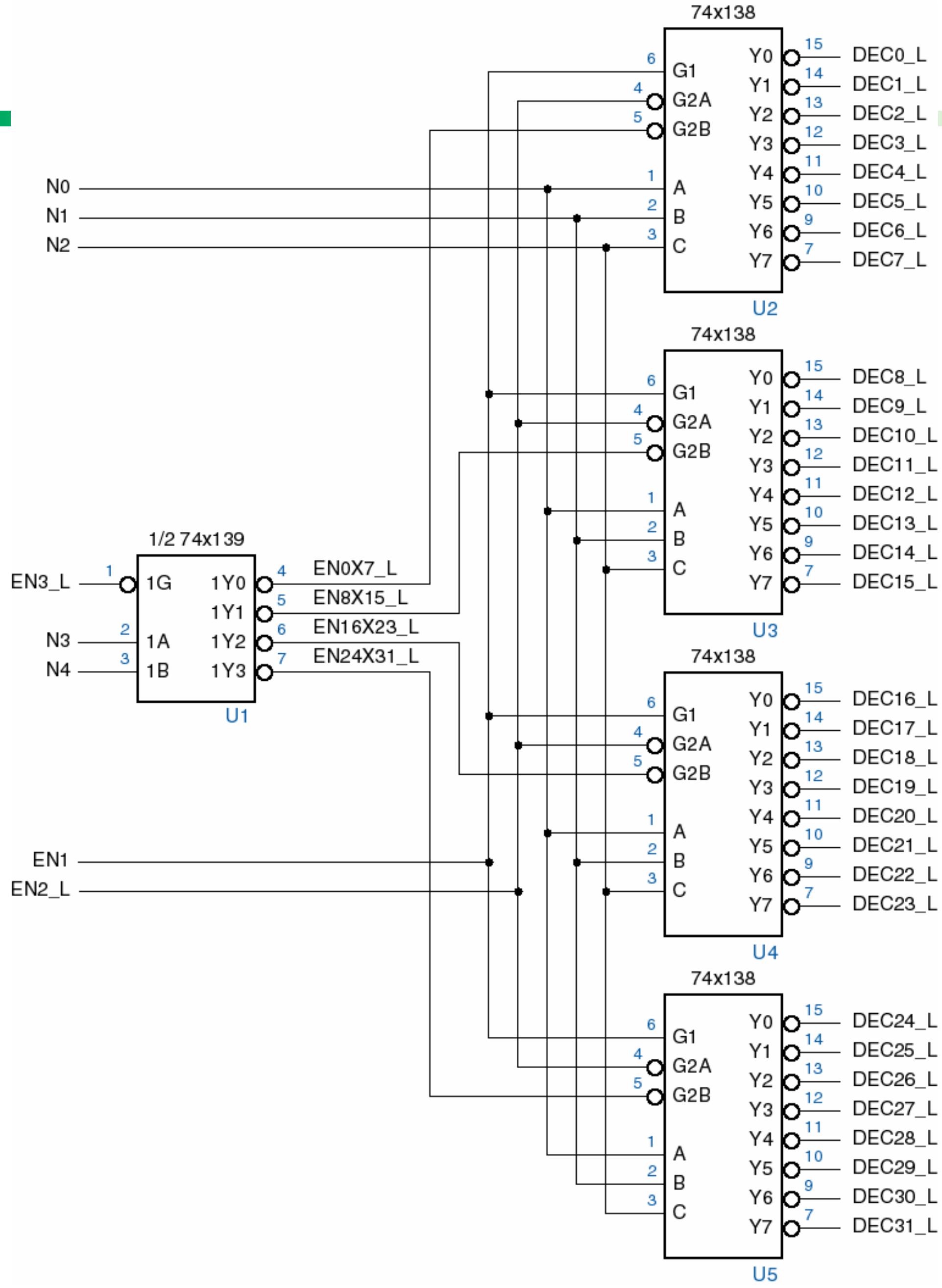


Decoder cascading



4-to-16 decoder

More cascading

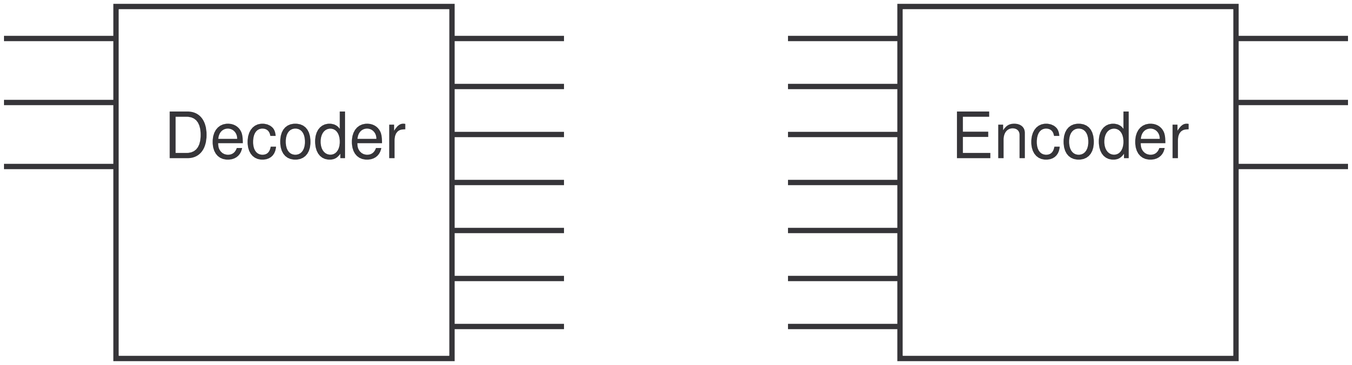


5-to-32 decoder

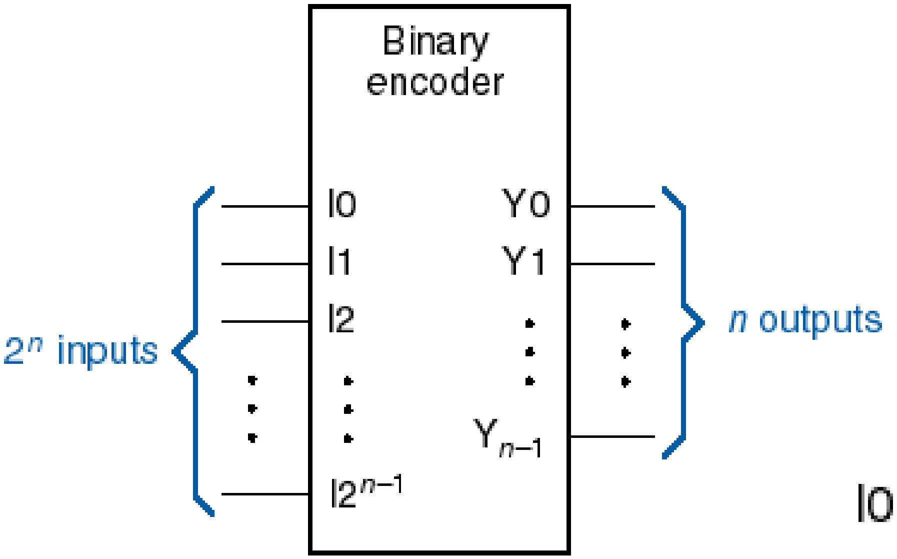
Decoder applications

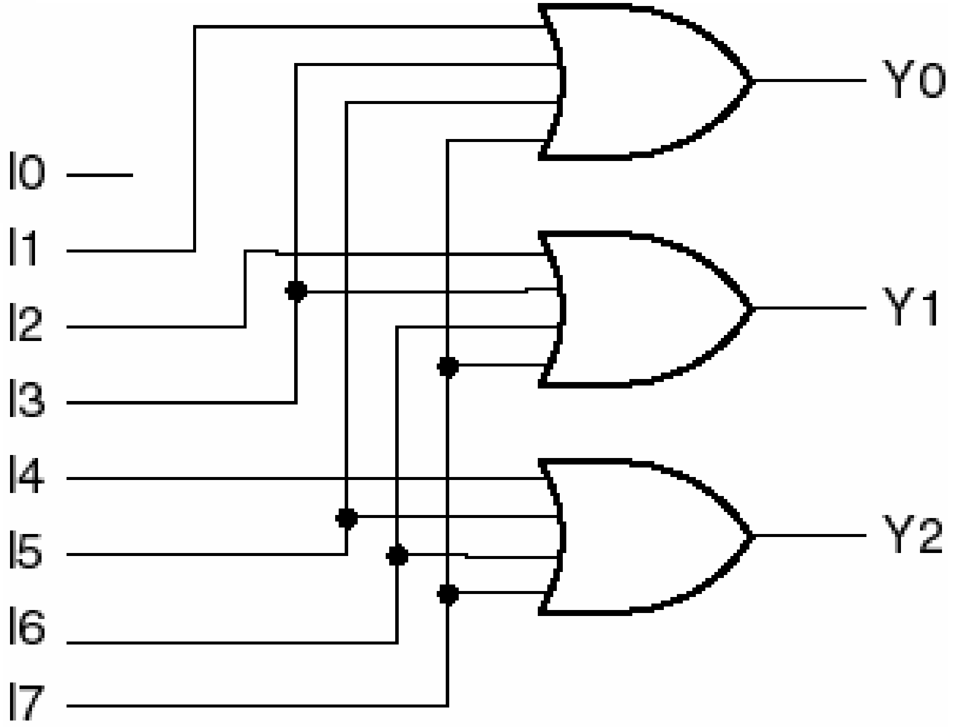
- Microprocessor memory systems
  - selecting different banks of memory
- Microprocessor input/output systems
  - selecting different devices
- Microprocessor instruction decoding
  - enabling different functional units
- Memory chips
  - enabling different rows of memory depending on address

Encoders vs. Decoders

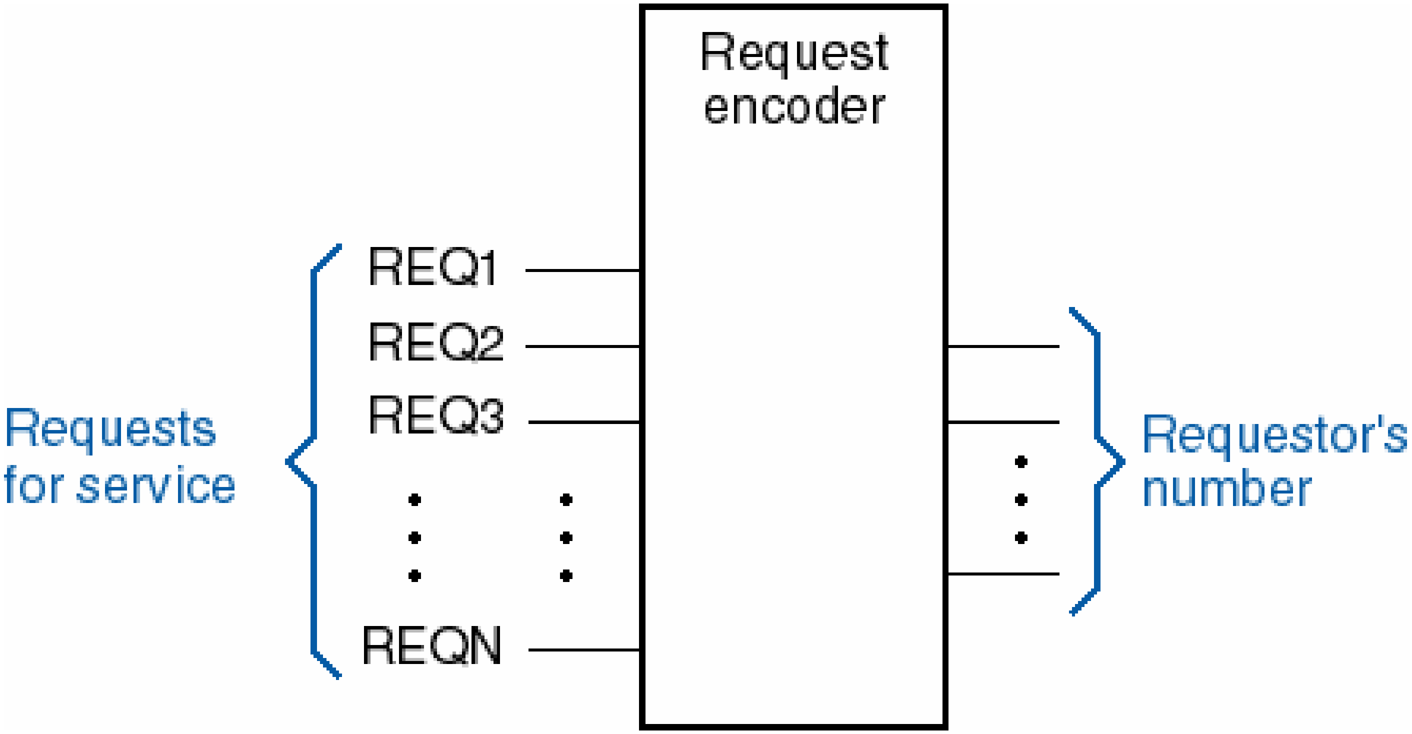


Binary encoders

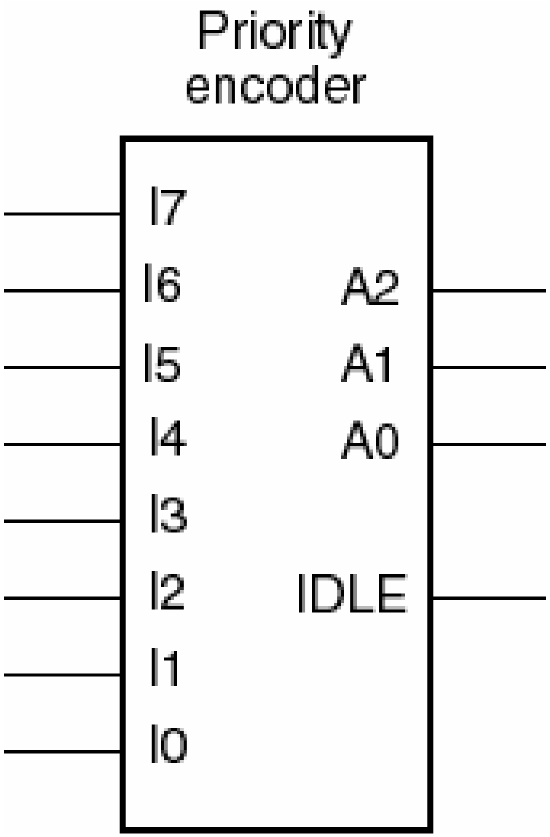




Need priority in most applications



8-input priority encoder



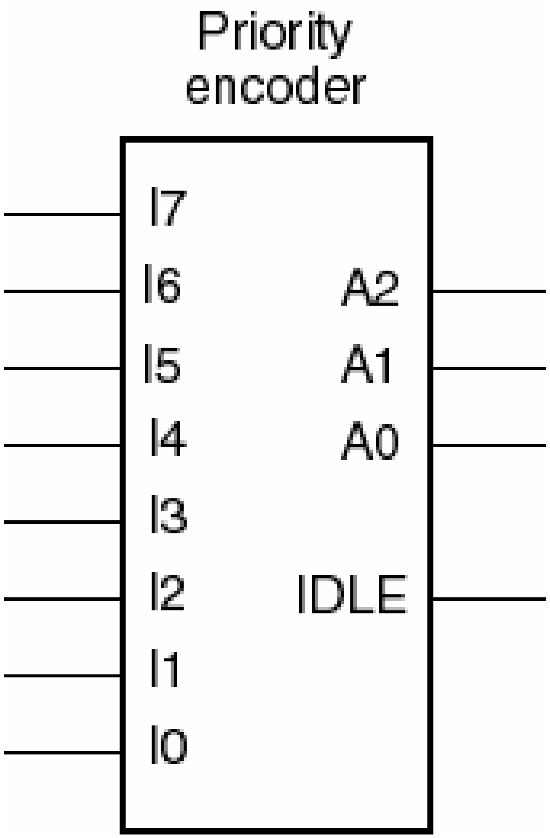
Priority-encoder logic equations

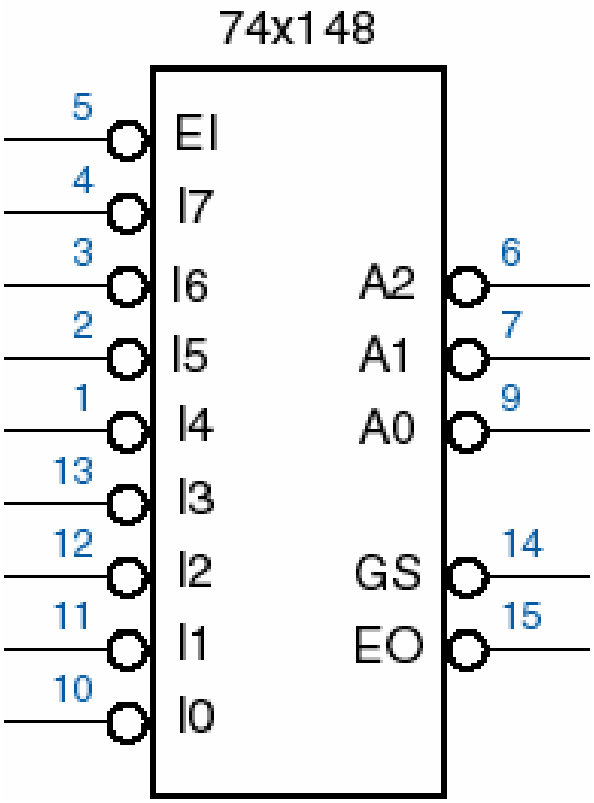
$$
\begin{aligned}
H7 &= I7 \\
H6 &= I6 \cdot I7' \\
H5 &= I5 \cdot I6' \cdot I7' \\
&\cdots \\
H0 &= I0 \cdot I1' \cdot I2' \cdot I3' \cdot I4' \cdot I5' \cdot I6' \cdot I7'
\end{aligned}
$$

$$
\begin{aligned}
A2 &= H4 + H5 + H6 + H7 \\
A1 &= H2 + H3 + H6 + H7 \\
A0 &= H1 + H3 + H5 + H7
\end{aligned}
$$

$$
\begin{aligned}
IDLE &= (I0 + I1 + I2 + I3 + I4 + I5 + I6 + I7)' \\
&= I0' \cdot I1' \cdot I2' \cdot I3' \cdot I4' \cdot I5' \cdot I6' \cdot I7'
\end{aligned}
$$

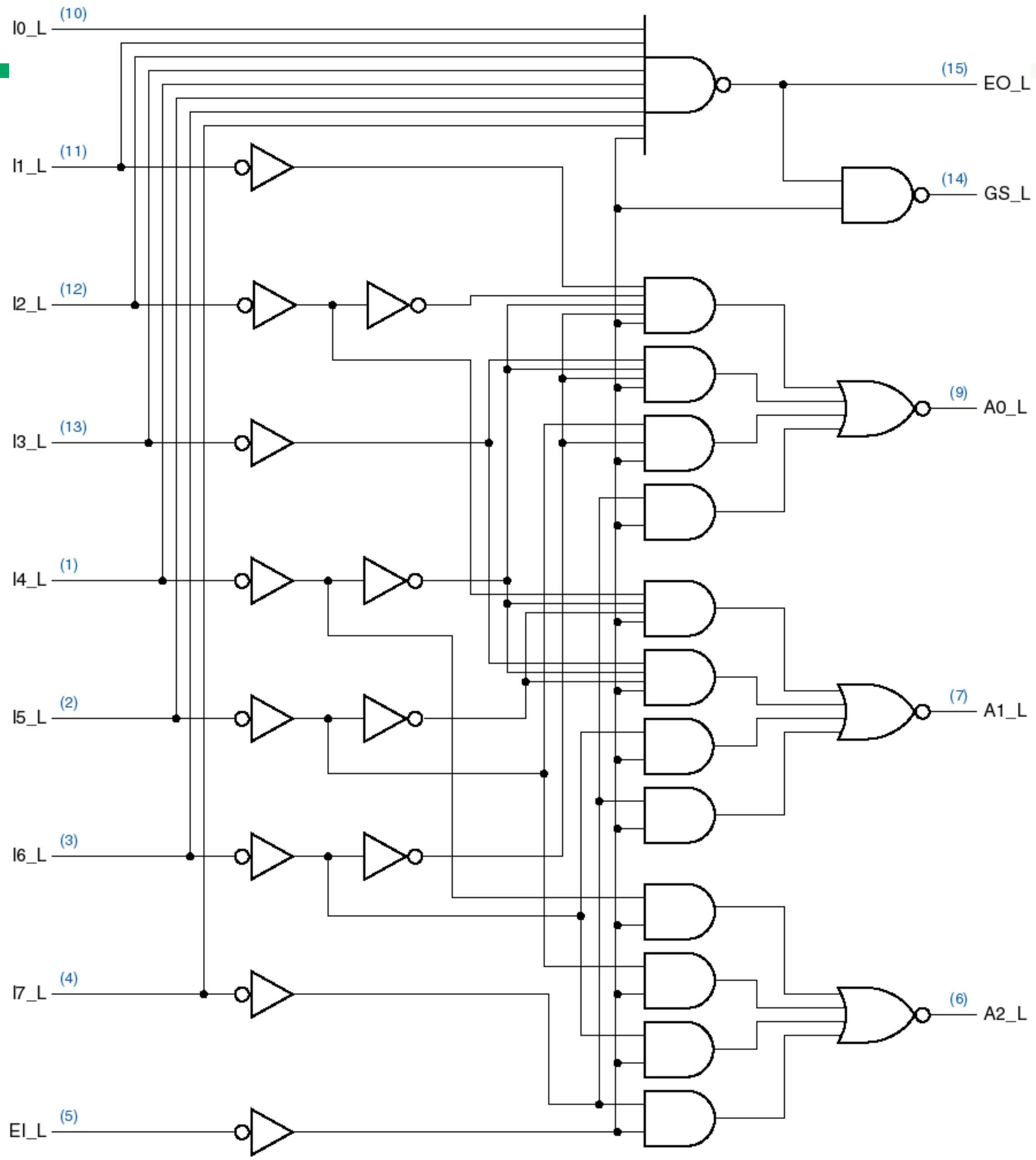
74x148 8-input priority encoder



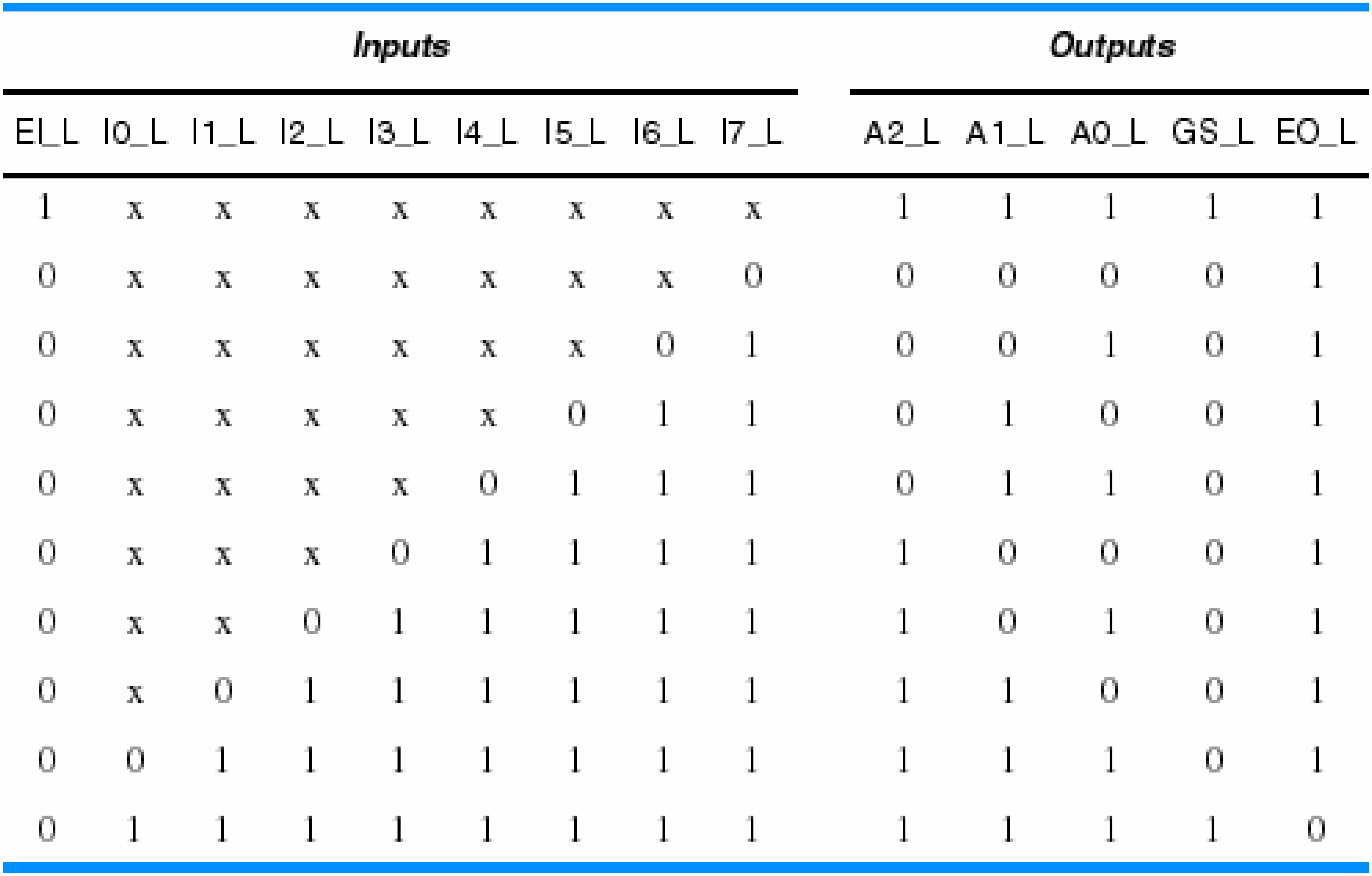


- Active-low I/O
- Enable Input
- “Got Something”
- Enable Output

74x148 circuit



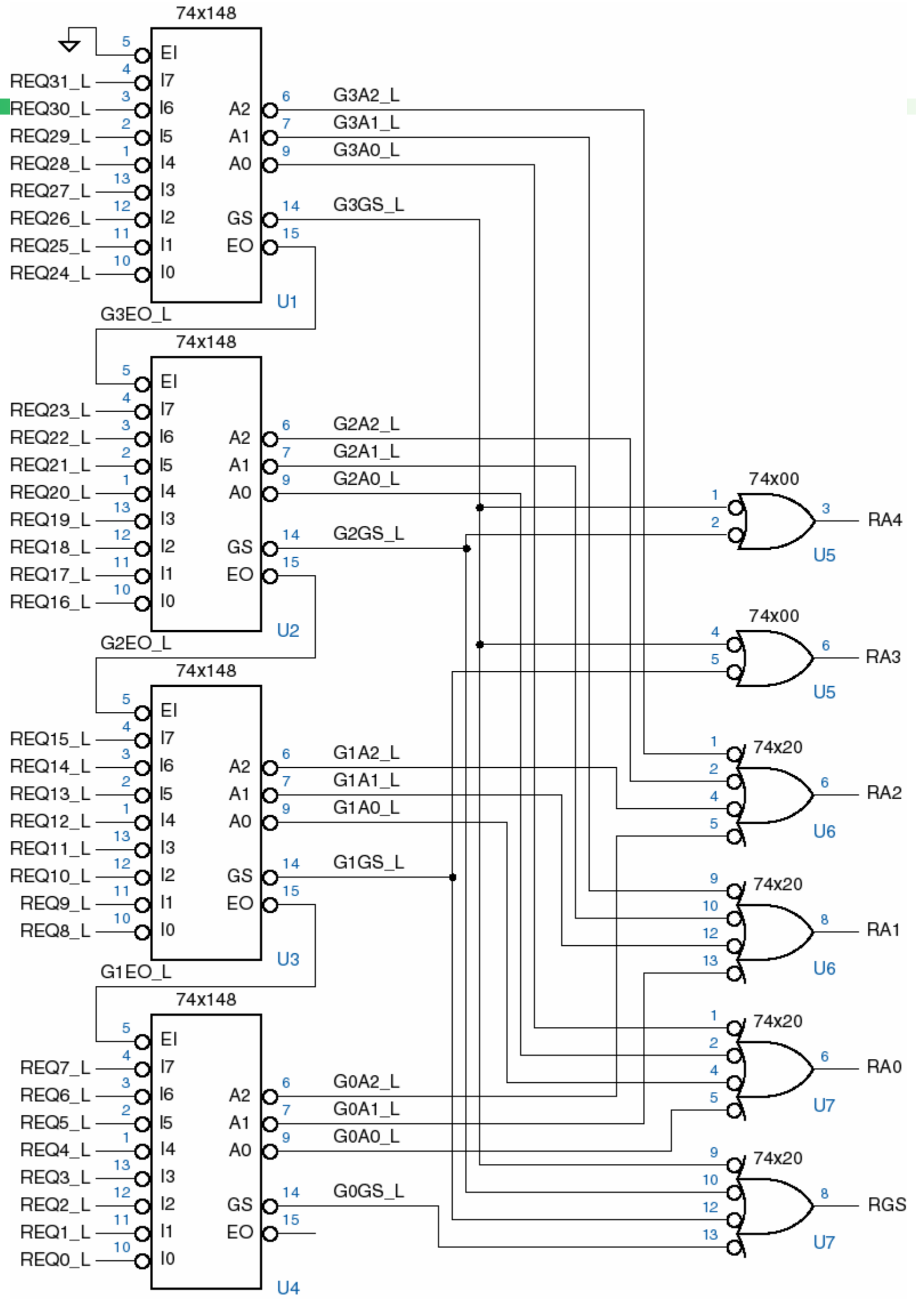
74x148 Truth Table



Inputs									*Outputs*				
EI_L	I0_L	I1_L	I2_L	I3_L	I4_L	I5_L	I6_L	I7_L	A2_L	A1_L	A0_L	GS_L	EO_L
1	x	x	x	x	x	x	x	x	1	1	1	1	1
0	x	x	x	x	x	x	x	0	0	0	0	0	1
0	x	x	x	x	x	x	0	1	0	0	1	0	1
0	x	x	x	x	x	0	1	1	0	1	0	0	1
0	x	x	x	x	0	1	1	1	0	1	1	0	1
0	x	x	x	0	1	1	1	1	1	0	0	0	1
0	x	x	0	1	1	1	1	1	1	0	1	0	1
0	x	0	1	1	1	1	1	1	1	1	0	0	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0

Cascading priority encoders

32-input
priority encoder


74x148
EI
I7
I6
I5
I4
I3
I2
I1
I0
A2
A1
A0
GS
EO
U1
U2
U3
U4
REQ31_L
REQ30_L
REQ29_L
REQ28_L
REQ27_L
REQ26_L
REQ25_L
REQ24_L
G3EO_L
REQ23_L
REQ22_L
REQ21_L
REQ20_L
REQ19_L
REQ18_L
REQ17_L
REQ16_L
G2EO_L
REQ15_L
REQ14_L
REQ13_L
REQ12_L
REQ11_L
REQ10_L
REQ9_L
REQ8_L
G1EO_L
REQ7_L
REQ6_L
REQ5_L
REQ4_L
REQ3_L
REQ2_L
REQ1_L
REQ0_L
G3A2_L
G3A1_L
G3A0_L
G3GS_L
G2A2_L
G2A1_L
G2A0_L
G2GS_L
G1A2_L
G1A1_L
G1A0_L
G1GS_L
G0A2_L
G0A1_L
G0A0_L
G0GS_L
74x00
U5
RA4
RA3
74x20
U6
RA2
RA1
U7
RA0
RGS