UNC Charlotte - ECGR2181 - Homework #11 - Due 4/25/06

Write a Verilog program for an ALU that satisfies the following requirements:

Req. 1: There are four 16-bit inputs: A, B, C and D. These are input data paths for the ALU.

Req. 2: There is one 16-bit output: OUT. This is the data path output for the ALU.

Req. 3: There is one 1-bit input: valid. When there is valid data and control signals and the ALU should provide a result, this signal will be raised to a "1". When it is "0", all outputs should be "0".

Req. 3: There are three 1-bit outputs: valid_out, cout, overflow. When valid = 1, valid out is =1. cout is the carry out value from the ADD and SUB operations. The overflow bit is set to 1 if the ADD or SUB operations result in an overflow.

Req. 5: There are two 2-bit inputs: Data1 and Data2. These are the selectors of the data (A, B, C, D) for the unary and binary operations. For unary operations, Data2 is ignored.

If datan=	Choose for data input
00	A
01	B
10	C
11	D

Req. 6: There is one 3-bit input: OP. This is the operation the ALU performs:

When OP=	Perform the operation, OUT=
000	Data1+Data2 (with carry)
001	Data1-Data2 (with borrow)
010	Data2-Data1 (with borrow)
011	-Data1 (negate)
100	Data1 & Data2
101	Data1 | Data2
110	(Data1)' (invert)
111	0xFFFF

Req. 7: This assignment is to be done using behavioral Verilog in a minimum amount of code.

Req. 8: The files should be complete and ready to use in the Xillinx ISE application. The first two lines will be comments that should look like the following (with your names in it and the correct file name).

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// ECGR2181 Homework 11 – filename:  alu.v
// Student's name – 4/25/06
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