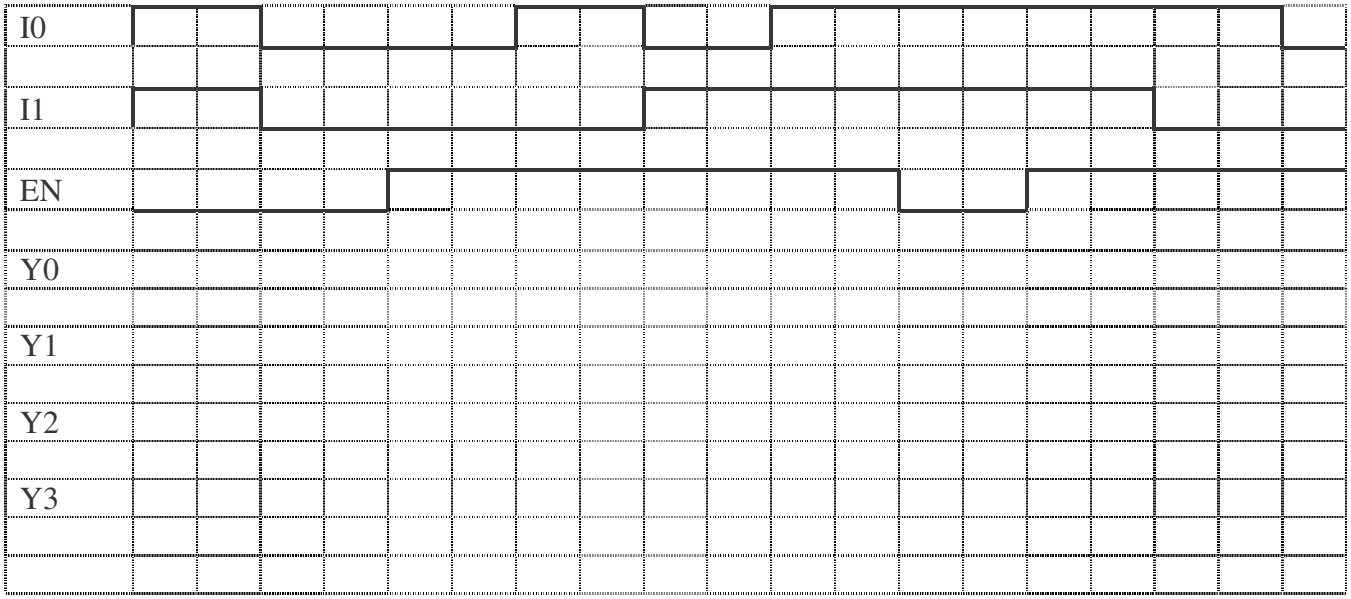
UNCC, Department of Electrical and Computer Engineering

ECGR 2181, Spring 2006, Lab #3, Due: 3/16/06, at the end of class (20 points)

Lab Partners: _____ and _____

Prelab:

1. Write the timing diagram for the decoder circuit with the following input (5 point)



In-class lab (3/16/06):

Using the knowledge learned from class and the previous lab exercise, implement via a schematic the 2 to 4 decoder from a VHDL file. You will use one of the VHDL files from Homework 7 to design the circuit, synthesize the circuit, and download the functionality to the FPGA board. Once you have completed the exercise, show the TA your work, then return the board. (5 points each)

NOTE: Use the labels above for the inputs, outputs. Choose your own switches and LEDs.

Show the TA your schematic. _____

Show the TA your working FPGA board showing the working decoder _____

Turn your board back in _____