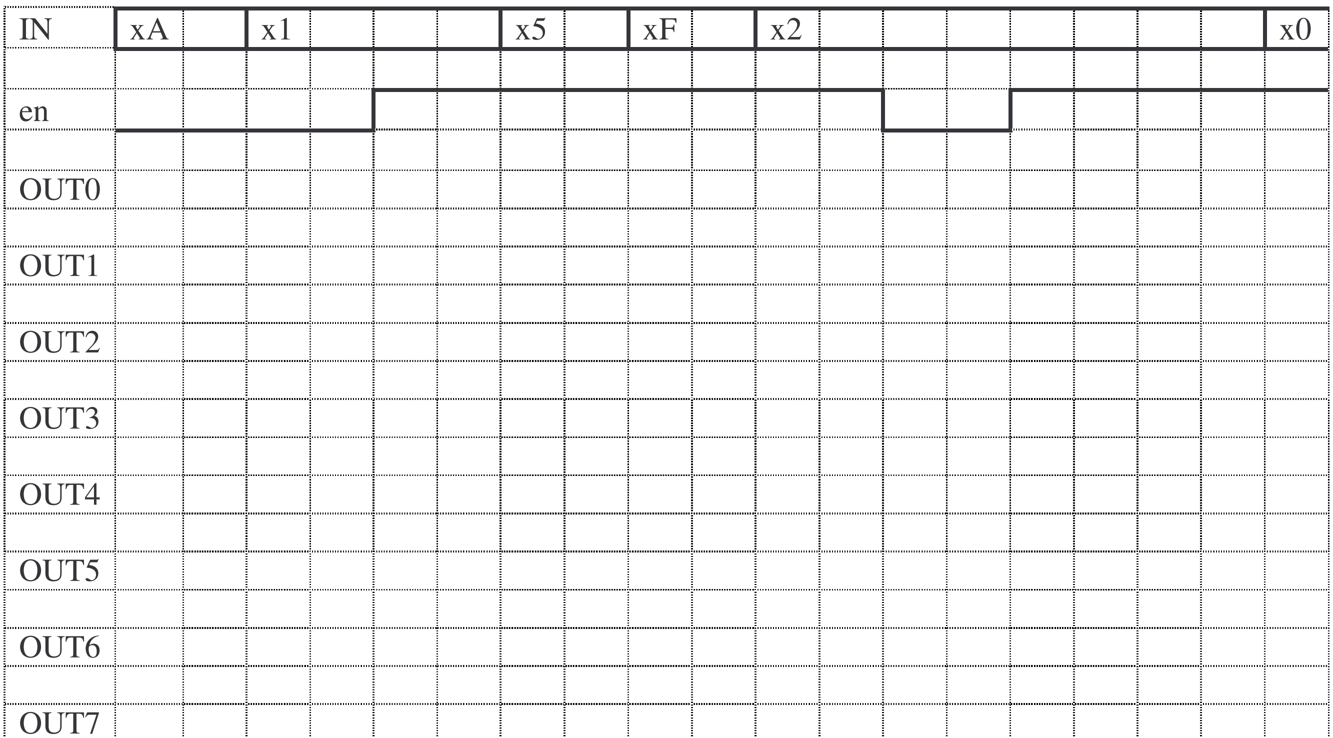
UNCC, Department of Electrical and Computer Engineering

ECGR 2181, Spring 2006, Lab #3, Due: 3/28/06, at the end of class (20 points)

Lab Partners: ______________________________ and ________________________________

Prelab:

1. Write the timing diagram for the decoder circuit with the following input (5 point)



In-class lab (3/28/06):

Using the knowledge learned from class and the previous lab exercise, implement via a behavioral model a 3 to 8 decoder from a Verilog file. You can modify one of the Verilog files from Homework 8 to design the circuit, synthesize the circuit, and download the functionality to the FPGA board. Once you have completed the exercise, show the TA your work, then return the board. (5 points each)

NOTE: Use the labels IN and en for the inputs; use OUT for the output. Choose your own switches and LEDs.

Show the TA your schematic. ________

Show the TA your working FPGA board showing the working decoder ________

Turn your board back in _________