UNC Charlotte - ECGR2181 – Lab 5 - Due 4/27/06

Lab Partners: _____ and _____

Prelab:

Write a Verilog program for an ALU that satisfies the following requirements:

Req. 1: There are two 4-bit inputs: A and B. These are input data paths for the ALU. A uses SW3 to SW0 with SW3 representing the MSB. B used SW7 to SW4 with SW7 representing the MSB.

Req. 2: There is one 4-bit output: OUT. This is the data path output for the ALU. This is represented by LEDs LD3 to LD0, with LD3 representing the MSB.

Req. 3: There are two 1-bit outputs: cout and overflow. cout (LD4) is the carry out value from the ADD and SUB operations. The overflow bit (LD7) is set to 1 if the ADD or SUB operations result in an overflow.

Req. 4: There is one 2-bit input which is made up of BTN1 and BTN0. This is the operation the ALU performs:

When BTN1 BTN0=	Perform the operation, OUT=
00	A+B (with carry)
01	A-B (with borrow)
10	A & B
11	A | B

Req. 5: Unlike the homework, the inputs are always valid (therefore there is no need for a "valid" input or output).

Req. 6: This assignment is to be done using behavioral Verilog in a minimum amount of code.

Req. 7: The file should be complete and ready to use in the Xillinx ISE application. The first two lines will be comments that should look like the following (with your names in it and the correct file name).

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// ECGR2181 Lab 5 - filename:  littlealu.v
// Student's name - 4/27/06
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In-class lab (5/27/06):

Req. 8: Create the project, synthesize the circuit, and download the functionality to the FPGA board. Once you have completed the exercise, show the TA your work. Return the FPGA Board.

Req. 9: One of your lab team must send the FINAL Verilog file to the TA Gajendra Singh (gsingh@uncc.edu) by 5:00 p.m. Thursday

Show the TA your working FPGA board showing the working decoder _____

Turn your board back in _____

FINAL Verilog File sent to Lab TA _____