UNC Charlotte - ECGR2181 – Lab 6 - Due 5/2/06

Lab Partners: _____ and _____

In-class lab (5/2/06):

You will be provided a file ALU.VHD that is a VHDL version of the Arithmetic and Logical Unit from Lab 5. You will build a test bench (not a waveform, like previously demonstrated) and simulate several example inputs. You are allowed 40 minutes for this exercise – NO MORE!

Steps:

1. Build a project using the provided VHDL file. (Note: The overflow functionality has not been provided – implementing the overflow is extra credit AFTER the rest of this has been done).
2. Create a VHDL test bench using the wizard. Hint: the inputs can be driven by statements like:
   - A<=”0010”;
   - B<=”1111”;
   - BTN<=”00”;
   - Wait for 100 ns between each set of input data.
3. Write the statements to verify the following data:
   - 3+3
   - 5-3
   - 5+5
   - -1 + 1
   - -5 + -5
   - F&4
   - 4|8
4. Run ModelSim and simulate the design. Once it has been successfully simulated, show the simulation to the TA.
5. Provide the test bench to the TA in an email later.

Show the TA your project workspace with the simulation _____

FINAL test bench file sent to Lab TA _____

EXTRA CREDIT: Overflow implemented _____ (shown during demo only)