Karnaugh-map usage

Plot 1s corresponding to minterms of function.

Circle largest possible rectangular sets of 1s.

- # of 1s in set must be power of 2
- OK to cross edges

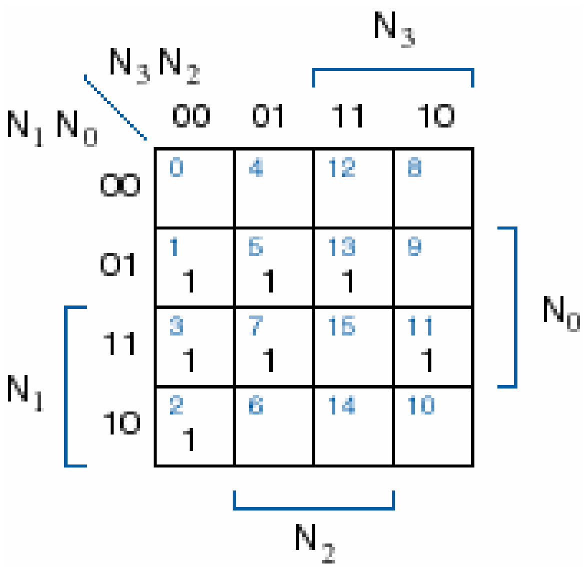
Read off product terms, one per circled set.

- Variable is 1 ==> include variable
- Variable is 0 ==> include complement of variable
- Variable is both 0 and 1 ==> variable not included

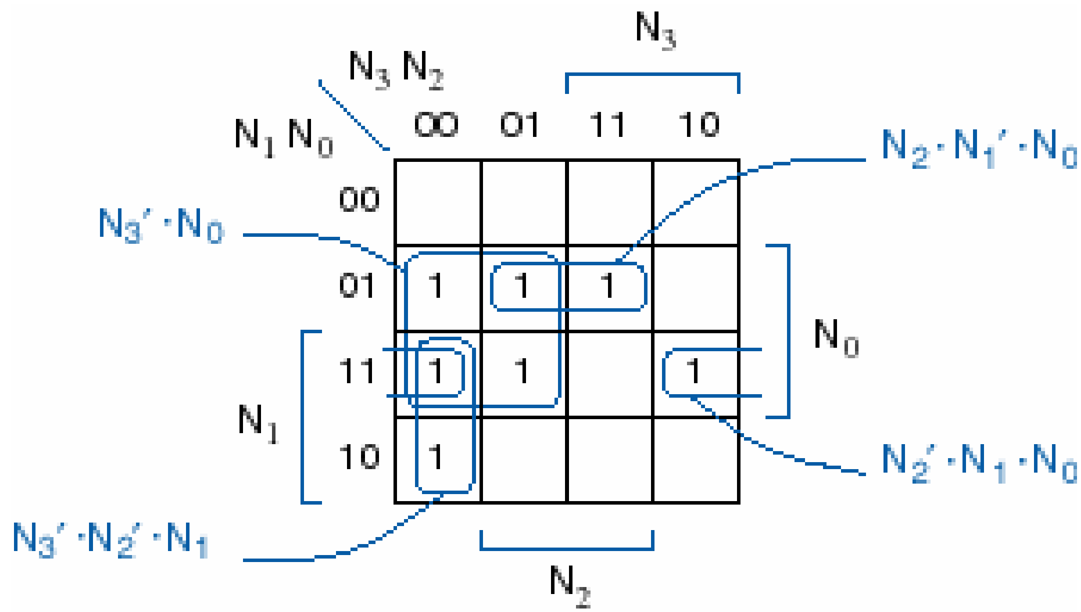
Circled sets and corresponding product terms are called "prime implicants"

Minimum number of gates and gate inputs

Prime-number detector

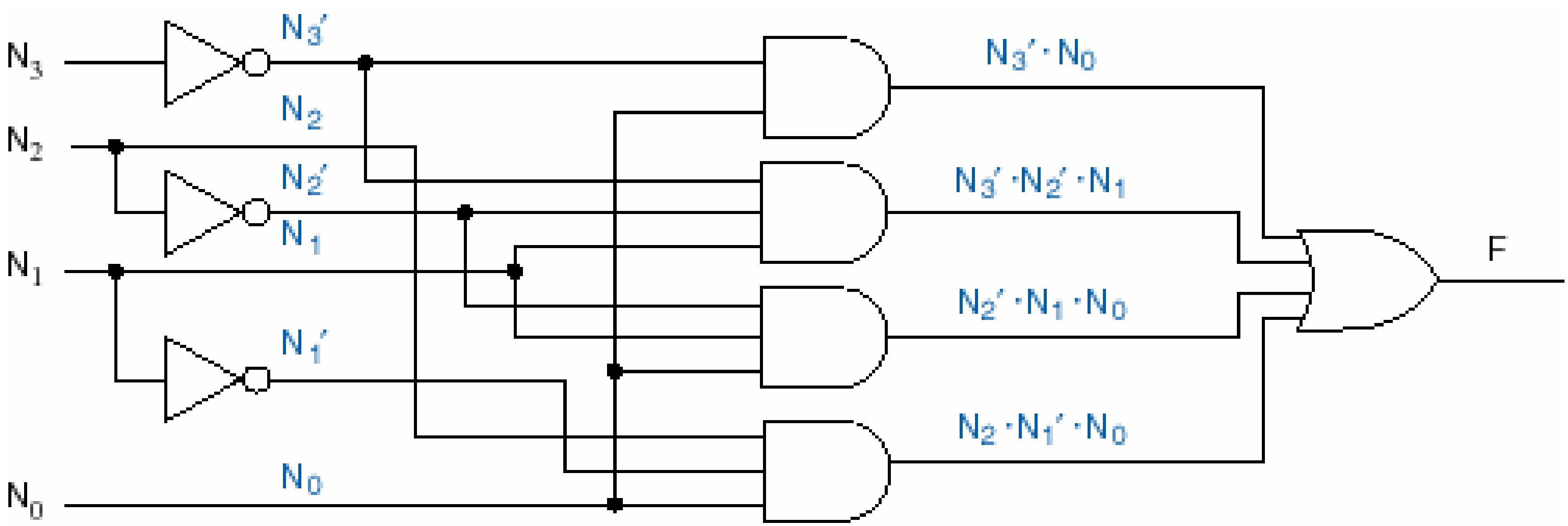


$F = \Sigma_{N3,N2,N1,N0}(1,2,3,5,7,11,13)$

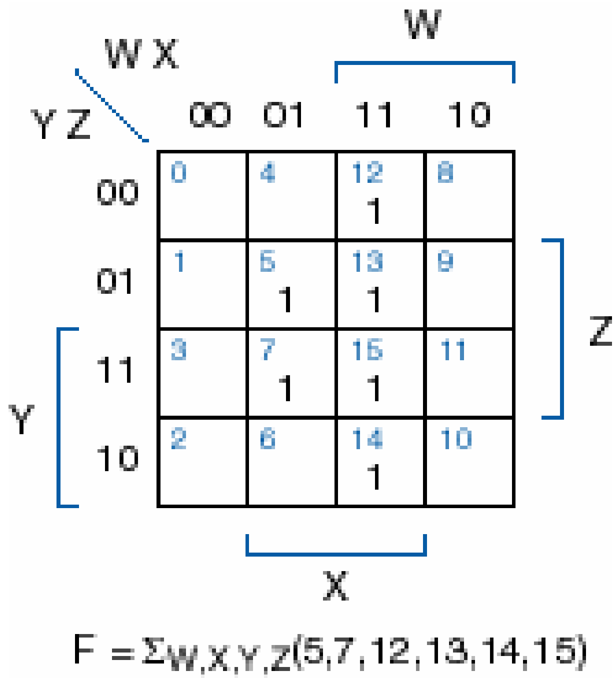


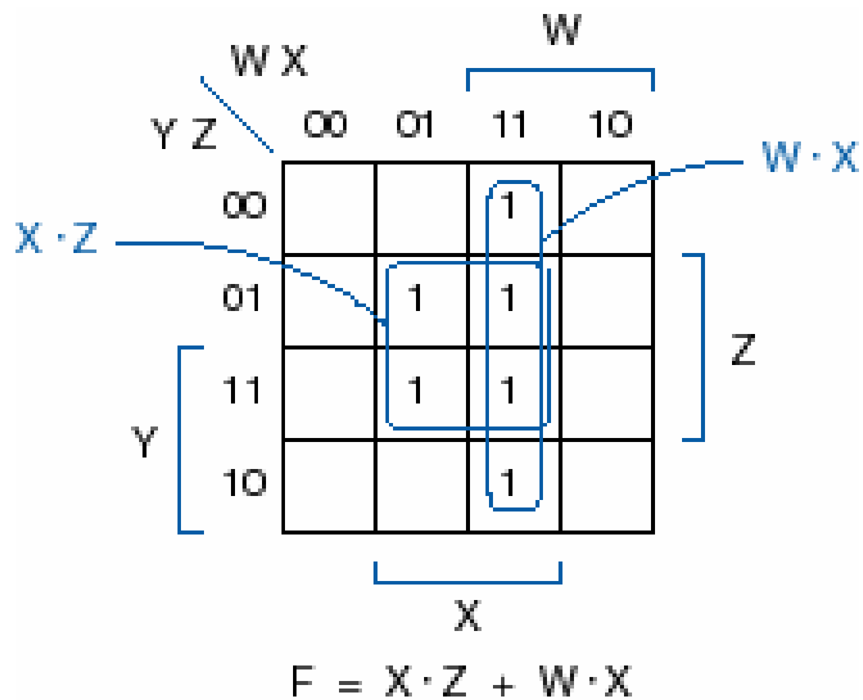
$F = N_3' \cdot N_0 + N_3' \cdot N_2' \cdot N_1 + N_2' \cdot N_1 \cdot N_0 + N_2 \cdot N_1' \cdot N_0$

Resulting Circuit.

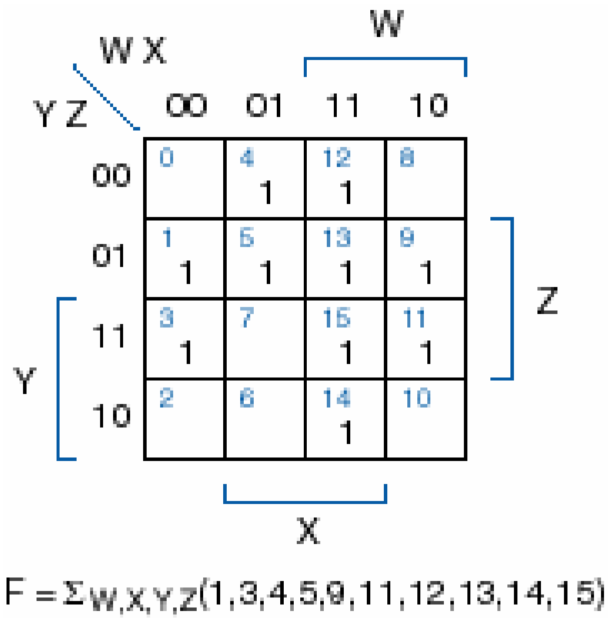


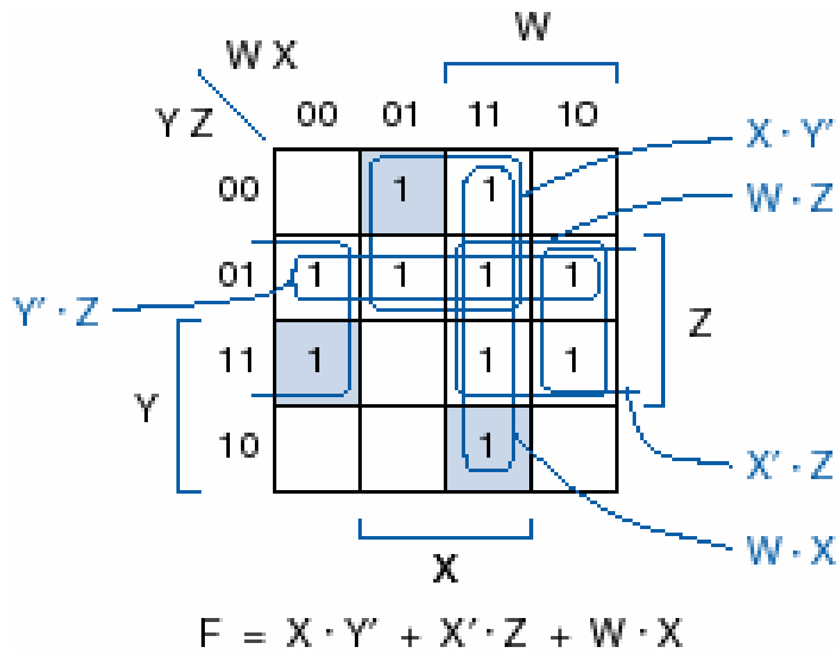
Another example





Yet another example



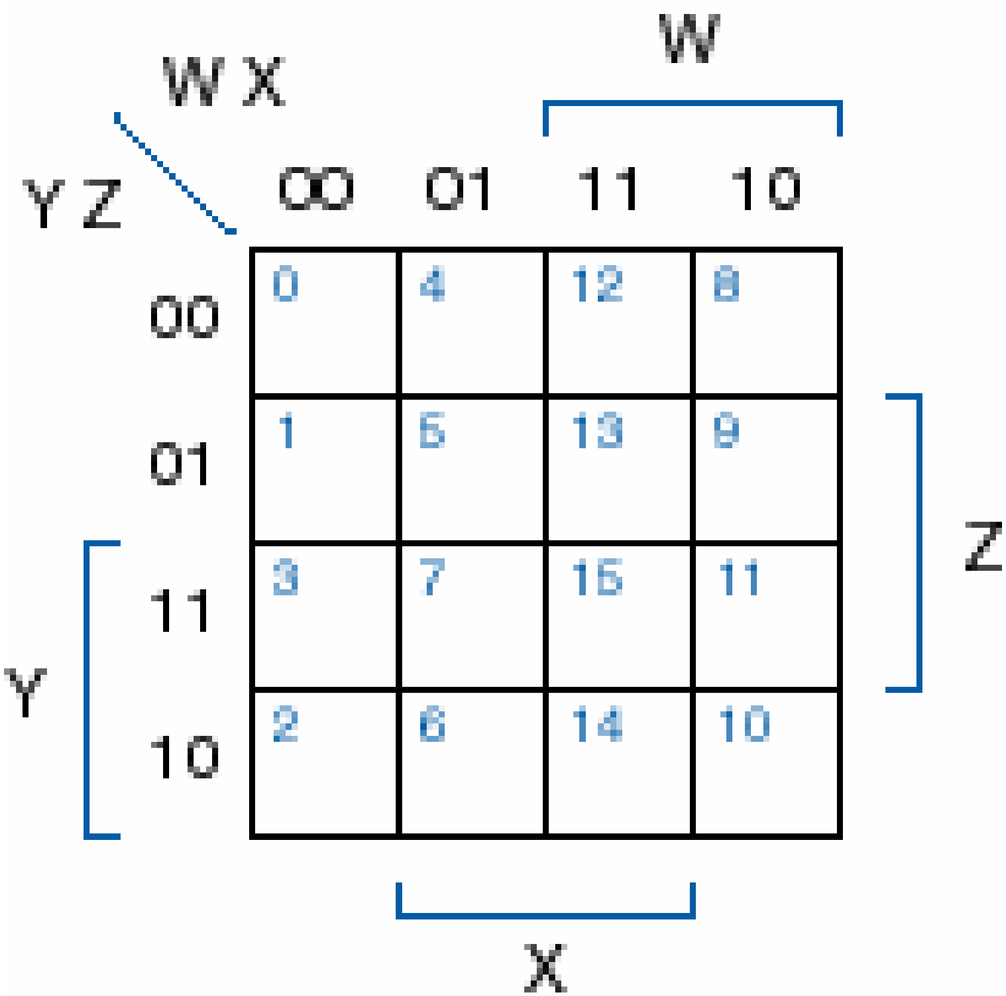


Distinguished 1 cells

Essential prime implicants

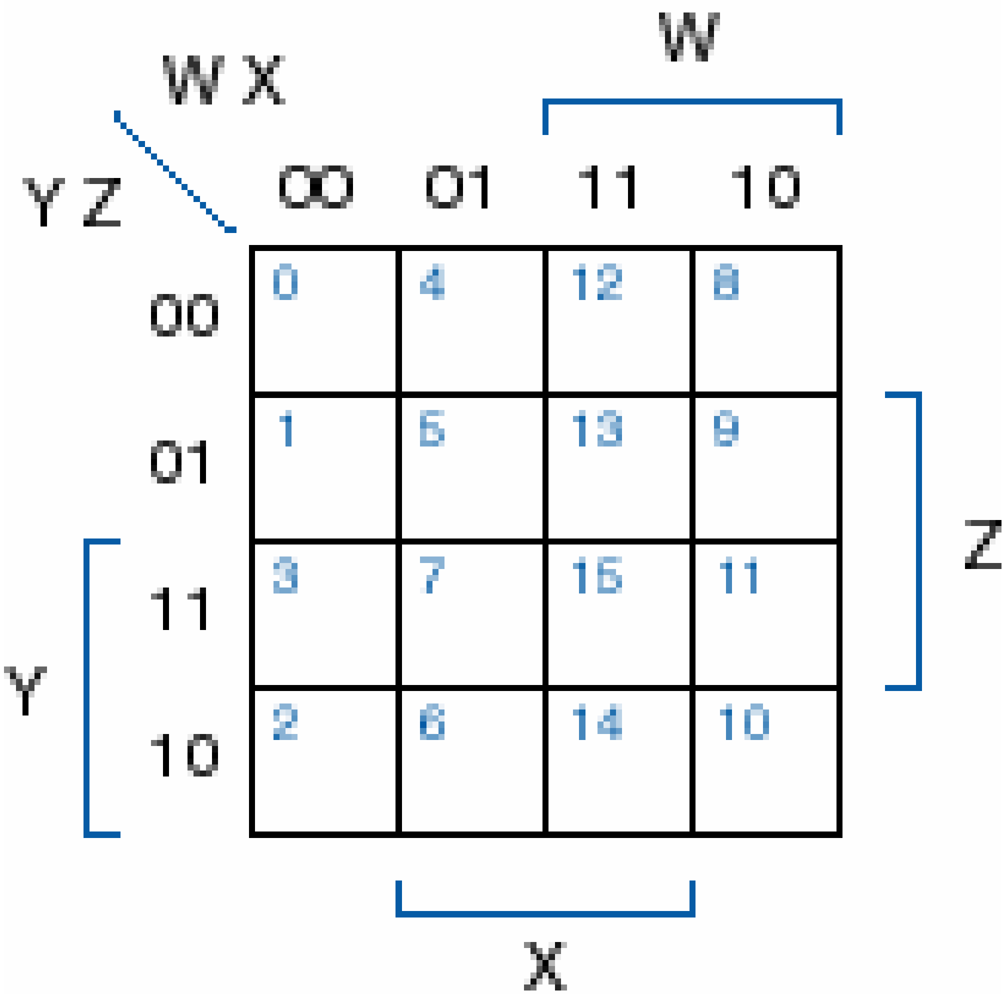
Another Example

$F(W,X,Y,Z) = \Sigma m(0,1,2,4,5,6,8,9,12,13,14)$



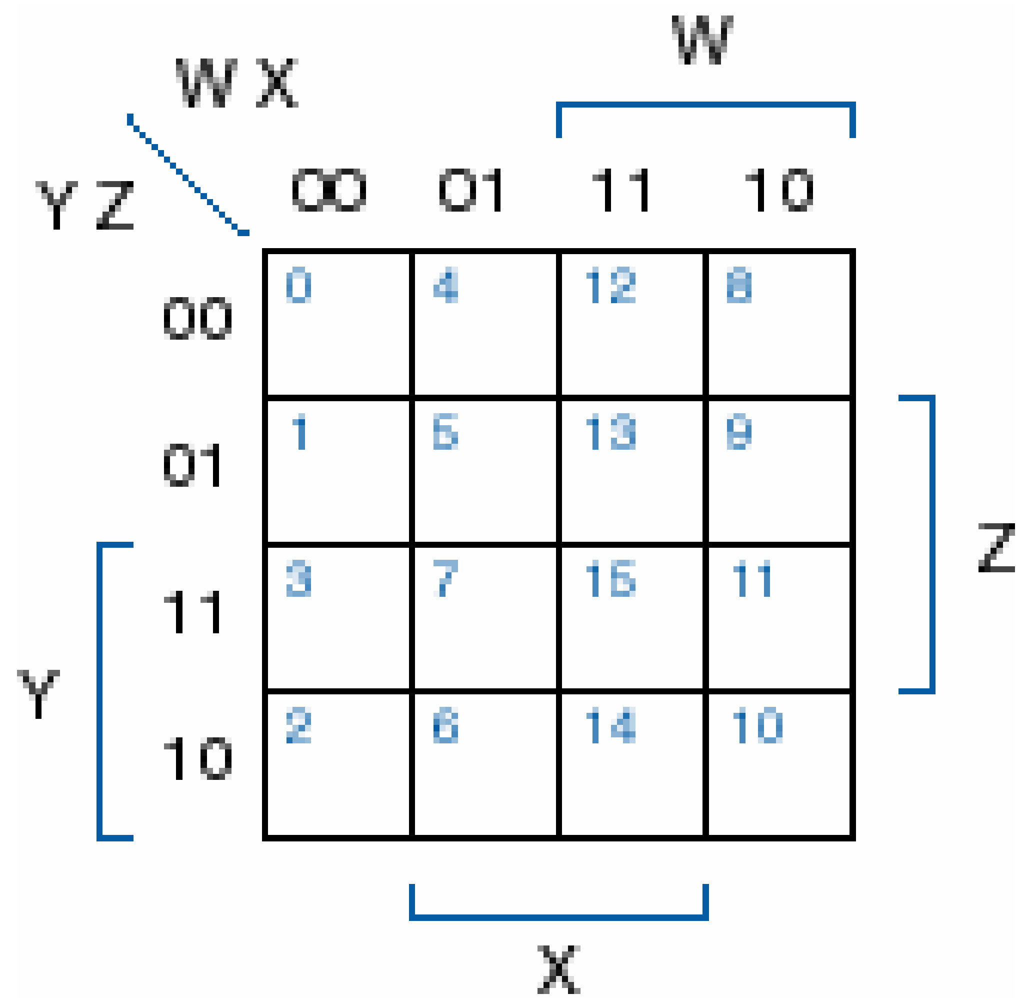
Another Example

$F(W,X,Y,Z) = \Sigma m(0,1,2,3,6,8,9,10,11,14)$



Another Example

$F(W,X,Y,Z) = \Sigma m(\qquad\qquad\qquad\qquad\qquad)$



Don’t Cares

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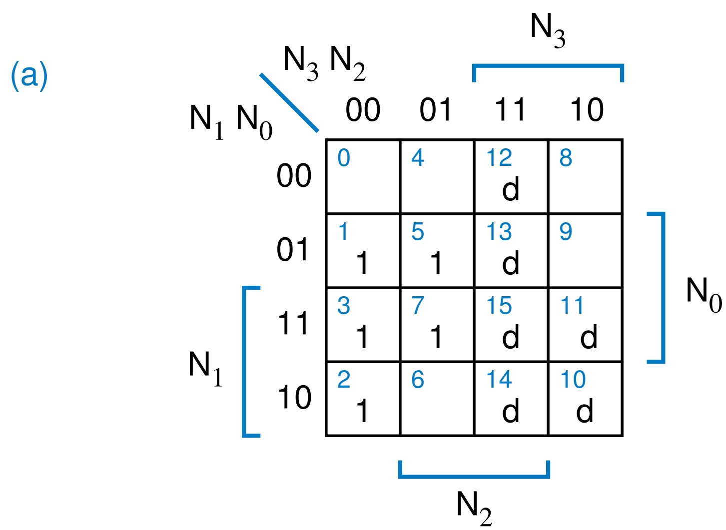
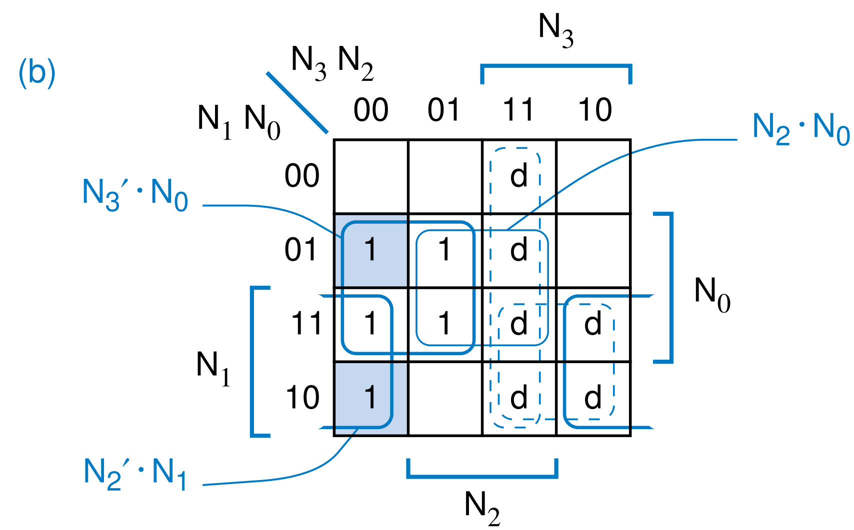


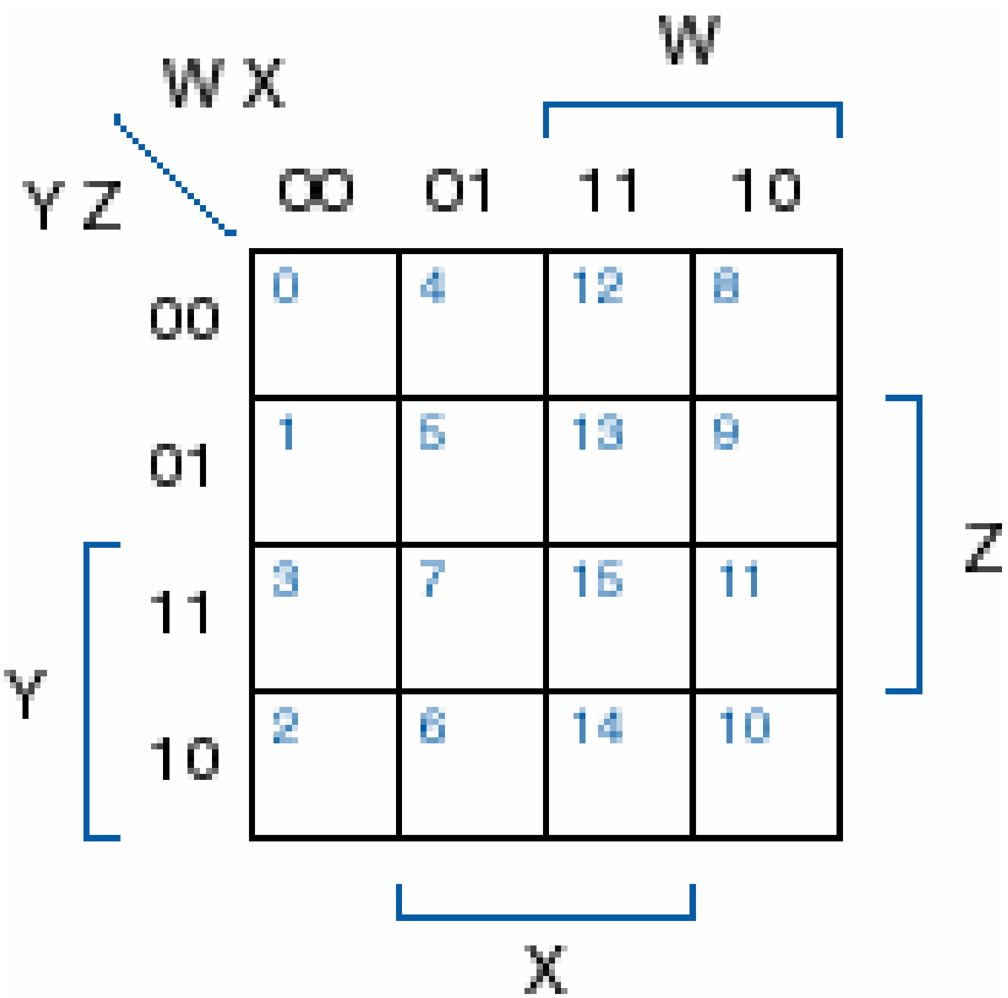
$F = \Sigma_{N3,N2,N1,N0}(1,2,3,5,7) + d(10,11,12,13,14,15)$



$F = N_3' \cdot N_0 + N_2' \cdot N_1$

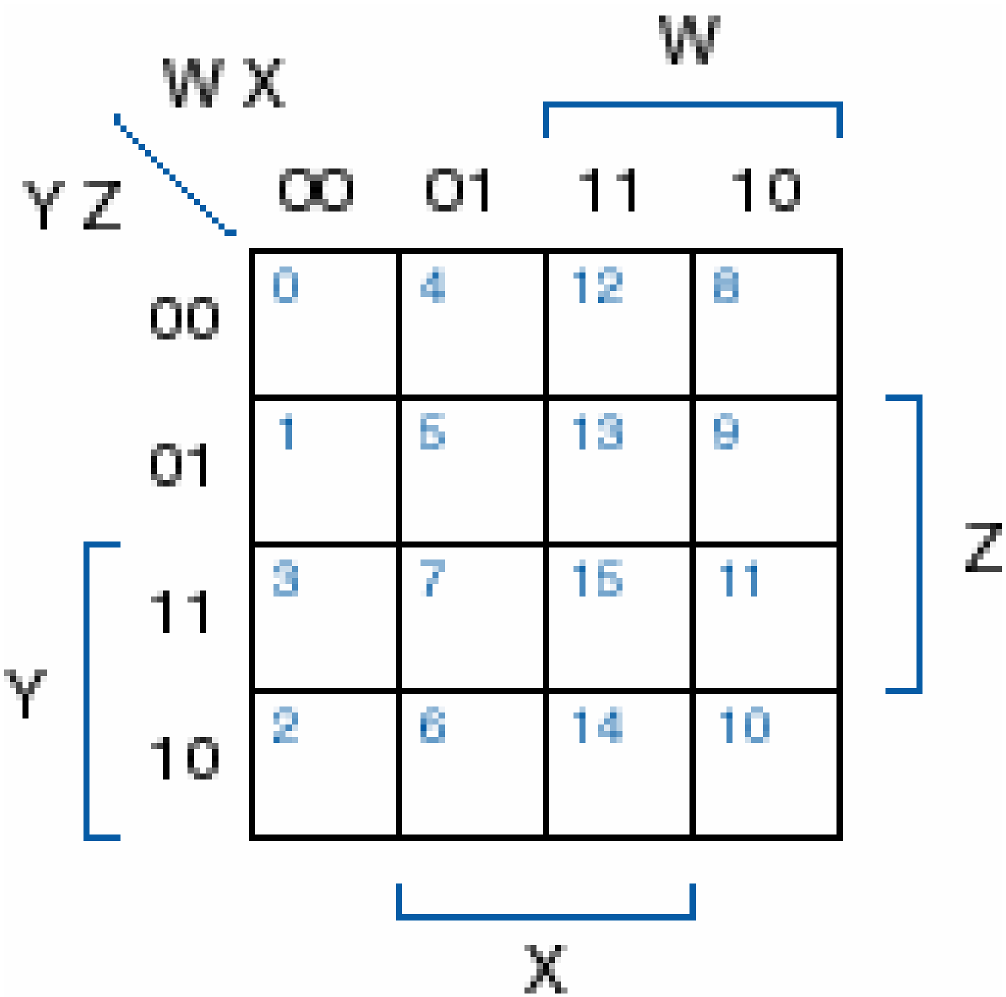
Another Example

$F(W,X,Y,Z) = \Sigma m(0,1,2,3,6,8,9,10,11,14) + d(7,15)$



Another Example

F(W,X,Y,Z) = Σm(   ) + d(   )

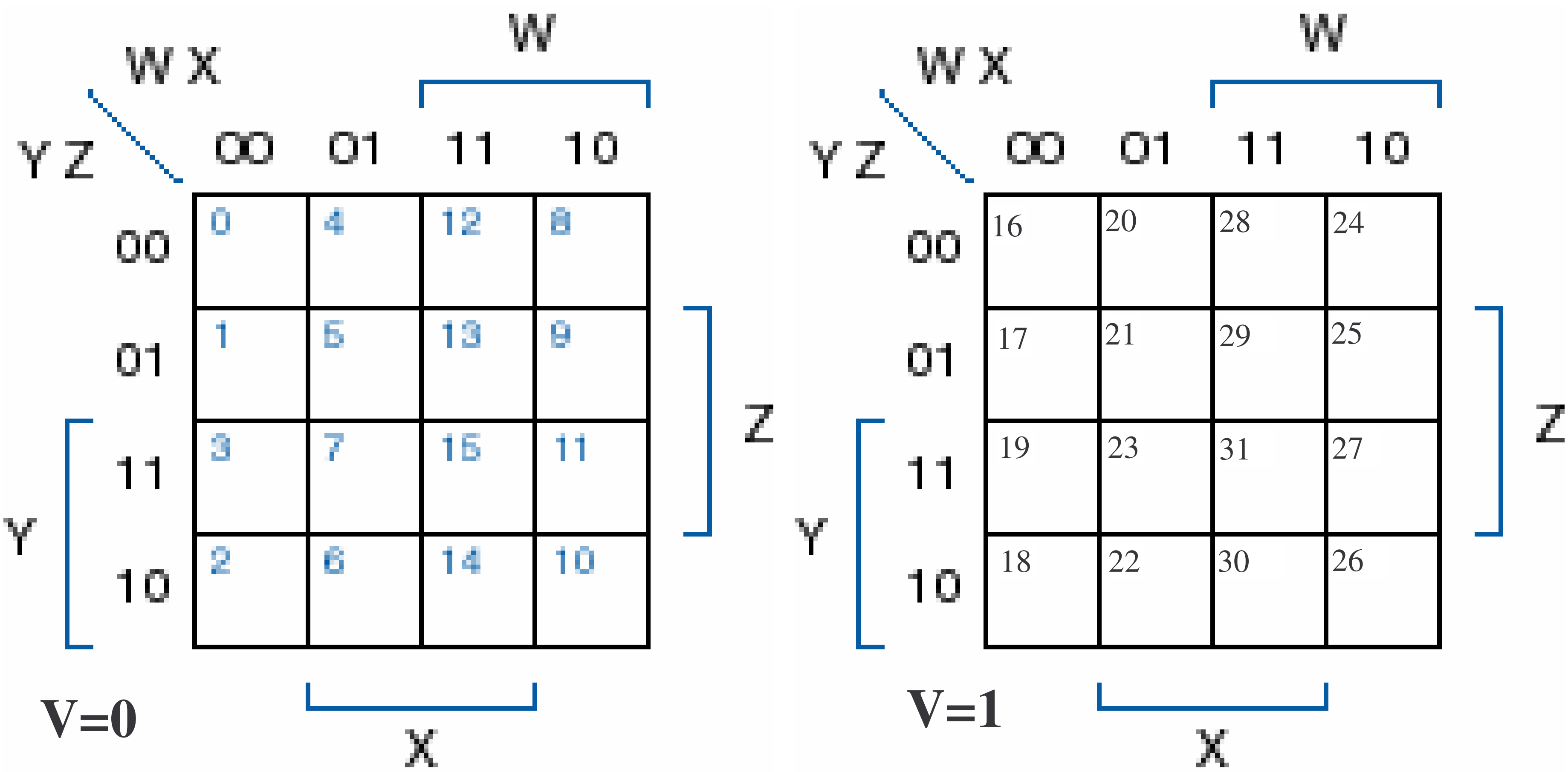


Resulting Circuit

$F(W,X,Y,Z) = \Sigma m(\qquad) + d(\qquad)$

Another Example

F(V,W,X,Y,Z) = Σm(0,1,2,3,16,17,18,19,20,21,22) + d(23,30,31)

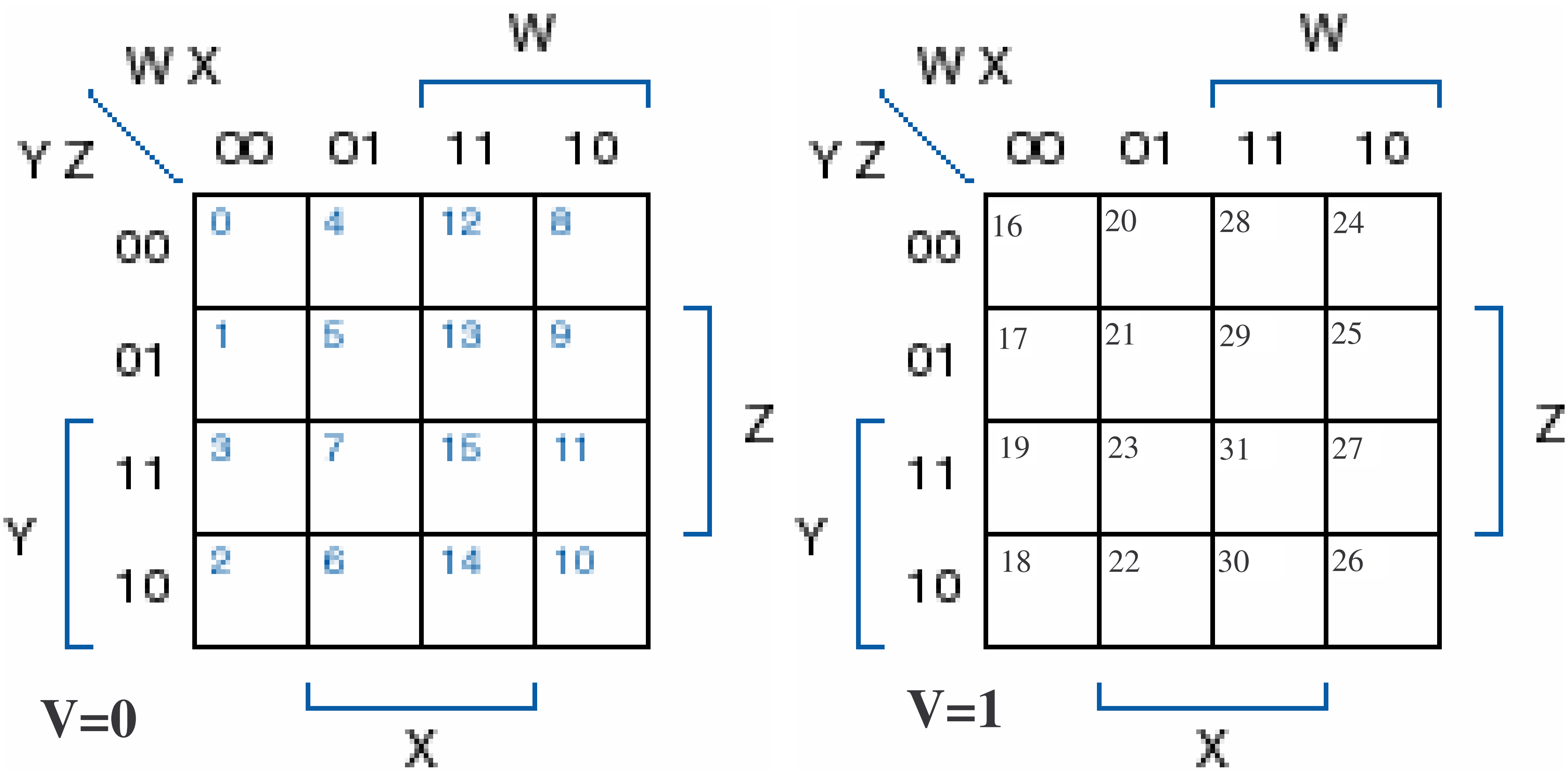


Resulting Circuit

$F(V,W,X,Y,Z) = \Sigma m(0,1,2,3,16,17,18,19,20,21,22) + d(23,30,31)$

Another Example

$F(V,W,X,Y,Z) = \Sigma m(\qquad) + d(\qquad)$



Current Logic Design

Lots more than 6 inputs -- can't use Karnaugh maps

Use software to synthesize logic expressions and minimize logic

Hardware Description Languages -- VHDL and Verilog