Introduction

The goal of this document is to walk the student through schematic entry using Xilinx ISE 7.1i; i.e., Xilinx FPGA design using schematic entry of logic diagrams. The Project Navigator, within ISE 7.1i, is the main interface through which FPGA design is accomplished. The basic topics covered are:

- Creating a project and adding source files,
- Project Navigator Overview,
- Editing a schematic source file,
- Assigning Package Pins,
- Synthesize the Design,
- Generate Programming File (.bit file),
- Configuring the Spartan-3 FPGA on the S3SK board, and
- Downloading and testing the project.

The Appendix will describe the step to create a module to use within other schematics in order to create a hierarchical design.

SPARTAN-3 Board

The student will utilize the Xilinx XC3S200 FPGA implemented on the SPARTAN-3 Starter Kit board by Digilent, Inc. Hereafter referred to as 'the Board' or 'S3SK board'. Make sure the Board is powered-up using the power cable. Also make sure the JTAG cable is connected, one end to the printer port on the PC and the other end to the JTAG port J7 on the SPARTAN-3 board. The signal names on the cable should be matched with the names silk-screened on the board while connecting the JTAG cable.

Project Description

This project implements a 2-input XOR gate. The slider switches SW5 and SW6 are used as inputs and LED (LD3) is used to observe the output. At the end of this project the Led will glow only if one of the switches is high (XOR function).

1. Creating a Project and Adding Source Files:

This section will describe starting a project for schematic design entry. First, lets look a the steps (or quick reference), then the explicit steps required are shown in pictorial form.

a. Quick Reference:

- Click **File** Menu and select **New Project**,
- A wizard (**New Project** Wizard) will appear to aide in setting up the project,
- Enter project name, select appropriate project location, set Top-Level Module Type to Schematic, then click **Next**,

- Describe the programmable device used for the project,
  - Device Family à Spartan3,
  - Device à xc3s200,
  - Package à ft256,
  - Speed Grade à -4, and
  - Leave the other options as defaulted.
- Click **Next**.

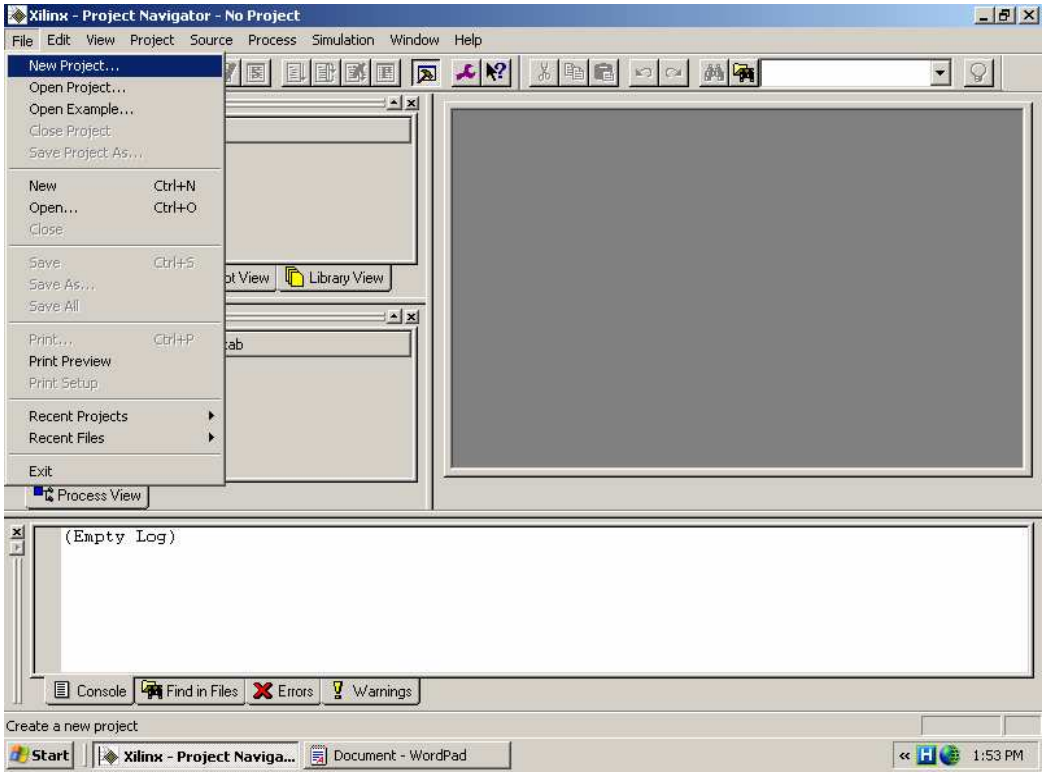
- Create New Source, click on **New Source** button,
- New Source dialog box will appear. The new source will be the top-level schematic,
- Enter File Name:, select Location (current project directory) and select Schematic as source type (large box to the left),
- Click **Next**, then **Finish**.

- Add Sources page will appear. Click **Next**, unless the student wants to add other preexisting sources.

- New Project Information page will appear. Confirm that the data was entered correctly, and then click **Finish**.

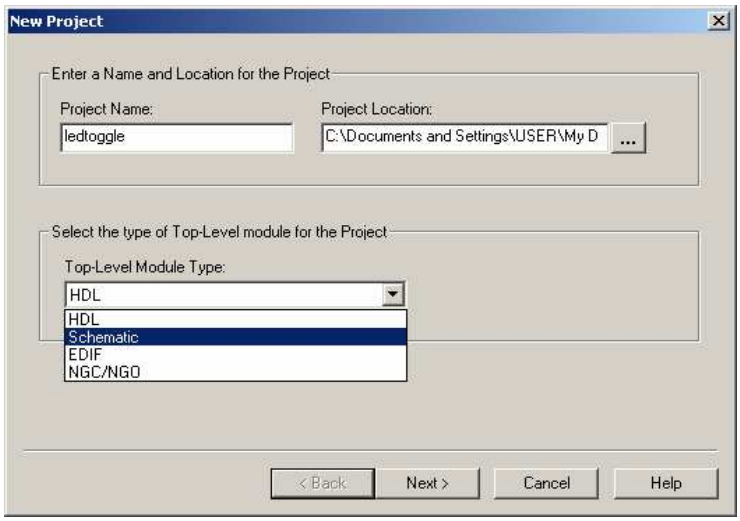
b. Creating Project Walk-through:

Open the Xilinx Project Navigator, then click on **File** menu and choose **New Project**

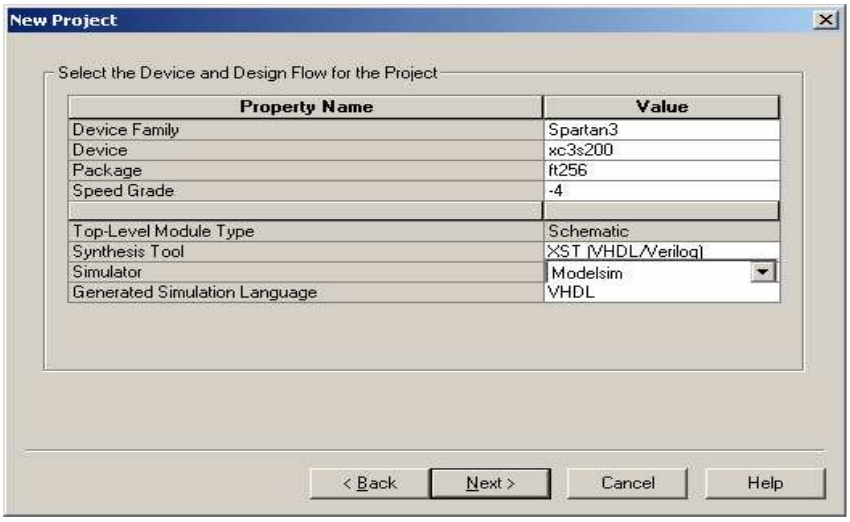


New Project window will appear as shown below.

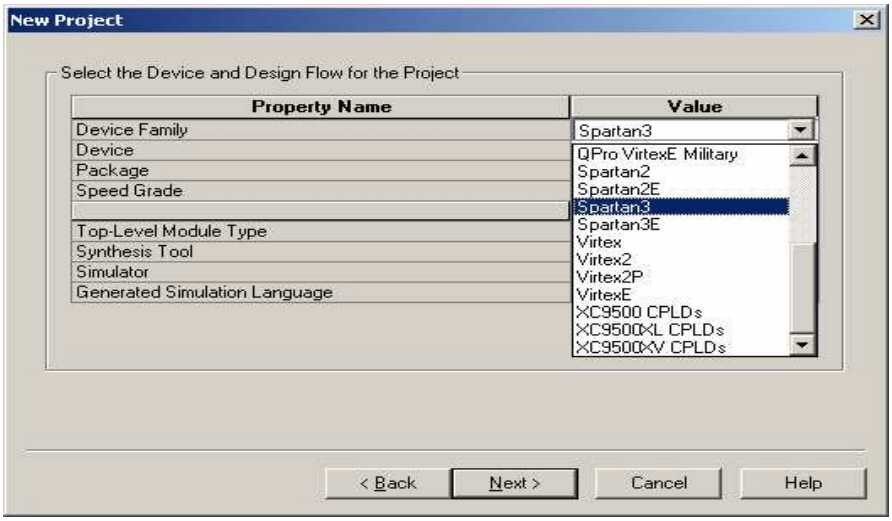
- Enter the project name (***ledtoggle)*** in the **Project Name** dialog box.
- Choose the project location by clicking on the button next to **Project Location** dialog box
- Choose the **Top-Level Module type** as one of four (HDL, Schematic, EDIF, NGC/NGO) as shown below. For this class, Schematic type is mostly going to be used. Choose **Schematic** and click **Next**.



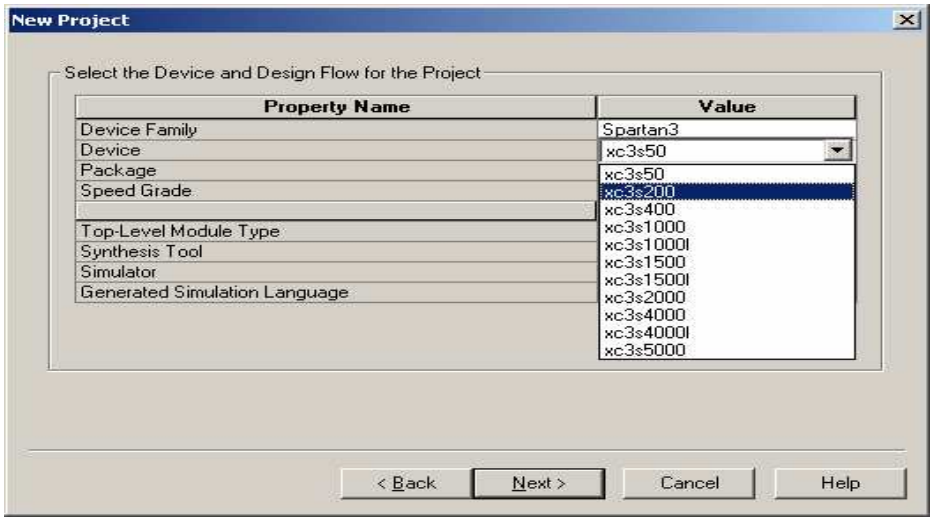
The following window for selecting the device and design flow will pop-up.



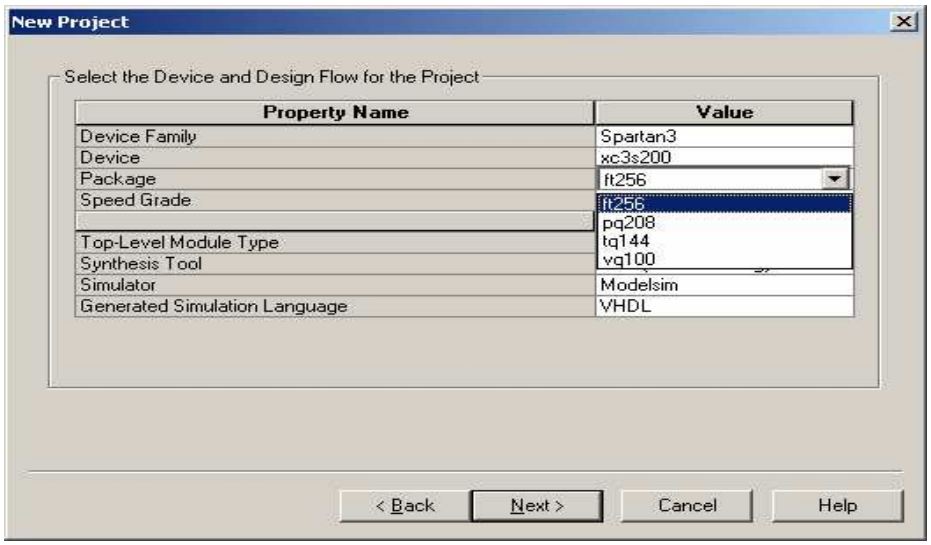
- For the Device Family select **Spartan3**



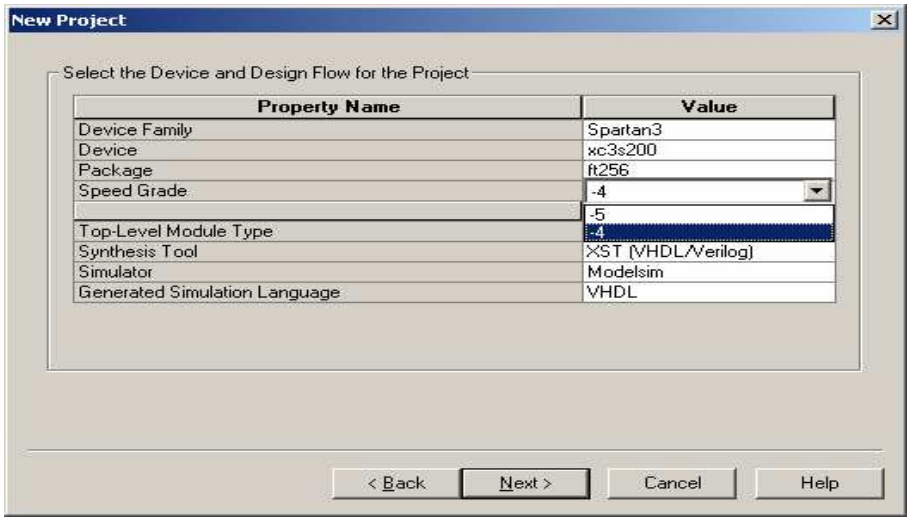
- For the Device select **xc3s200**



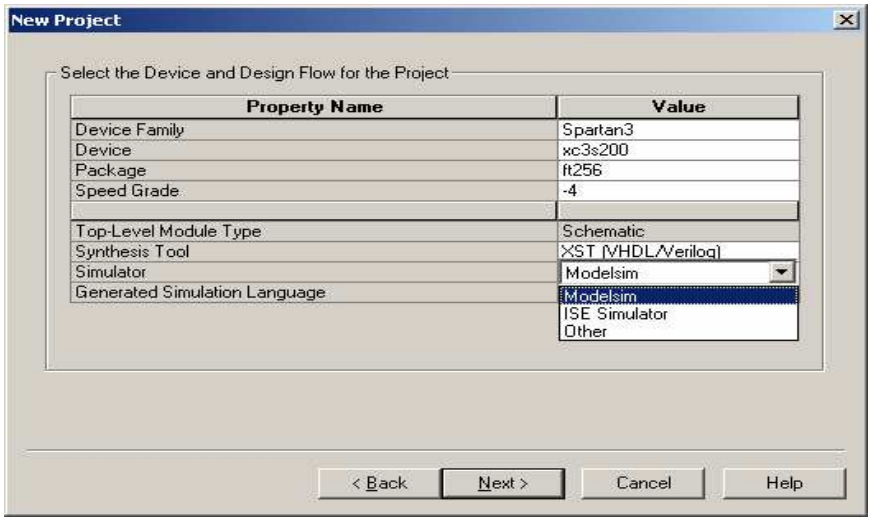
- For Package select **ft256**



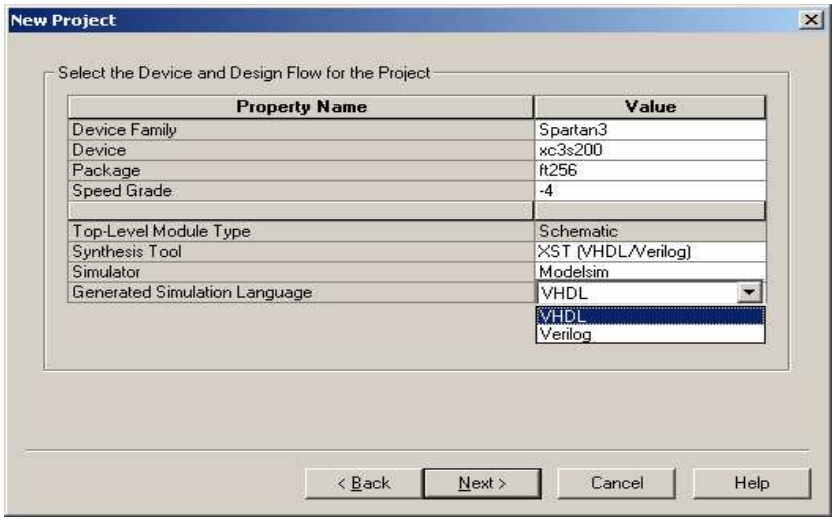
- For Speed Grade select **-4**



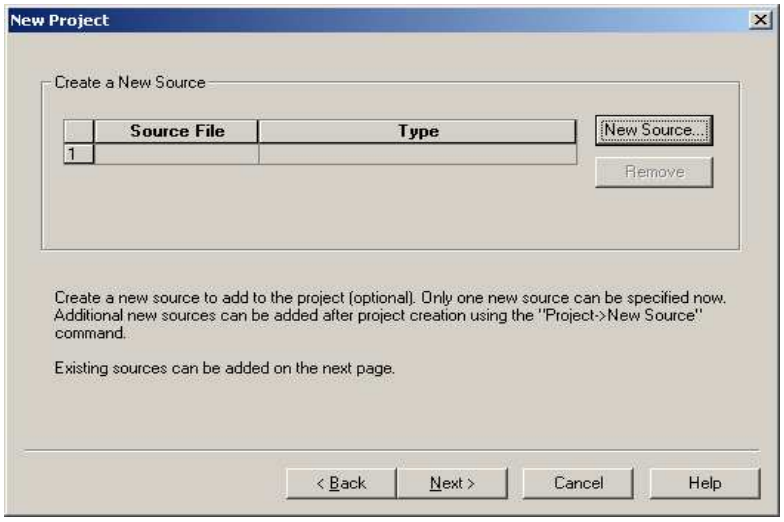
- For Simulator select **Modelsim**



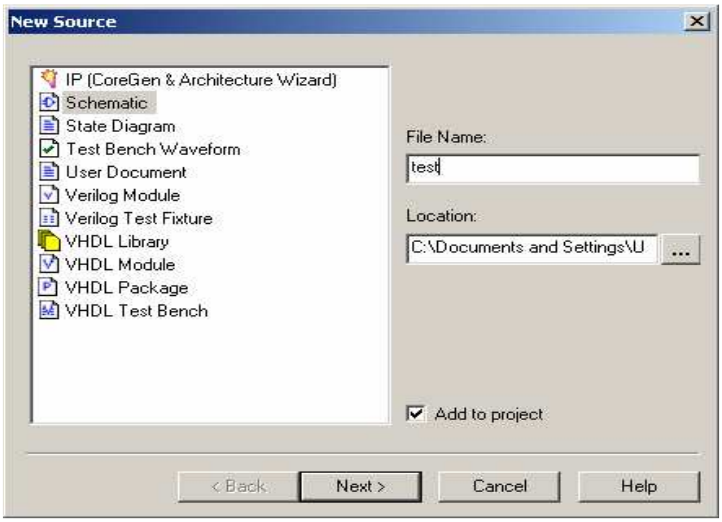
- Finally **VHDL** for Generated Simulation Language and click **Next**



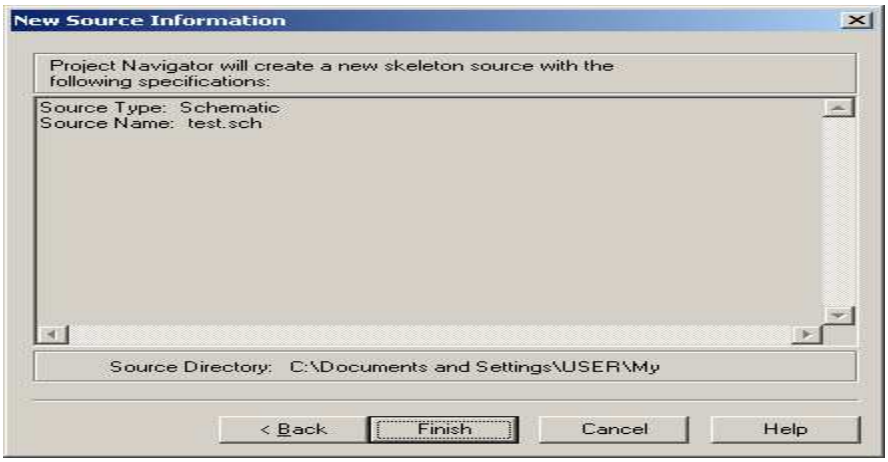
- Source file window will pop-up. Click on the **New Source** button. This new source will become the Top-Level Schematic.



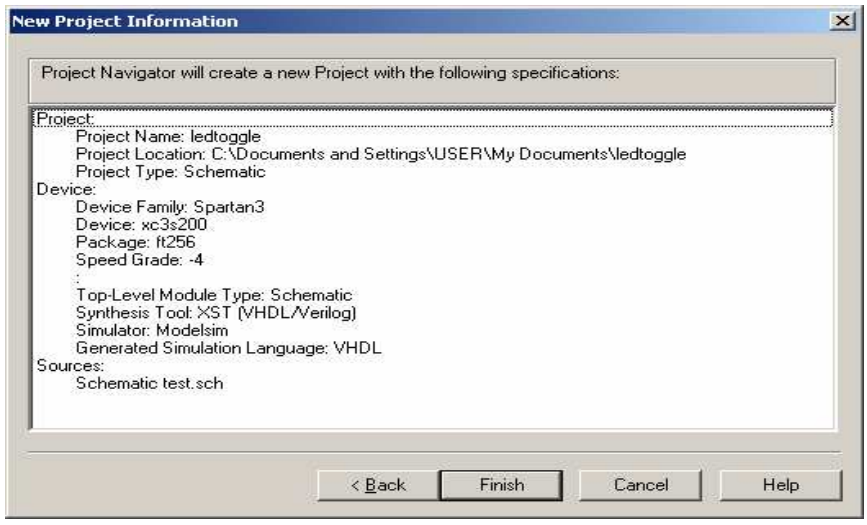
- In the New Source window select **Schematic** and enter the File Name. For current example, schematic file name is given as ***test.*** Choose the file location by clicking the button next to **Location** dialog box. Check the box before the **Add to Project** if not already checked and click **Next.**



- The source info window will pop-up. Click **Finish**



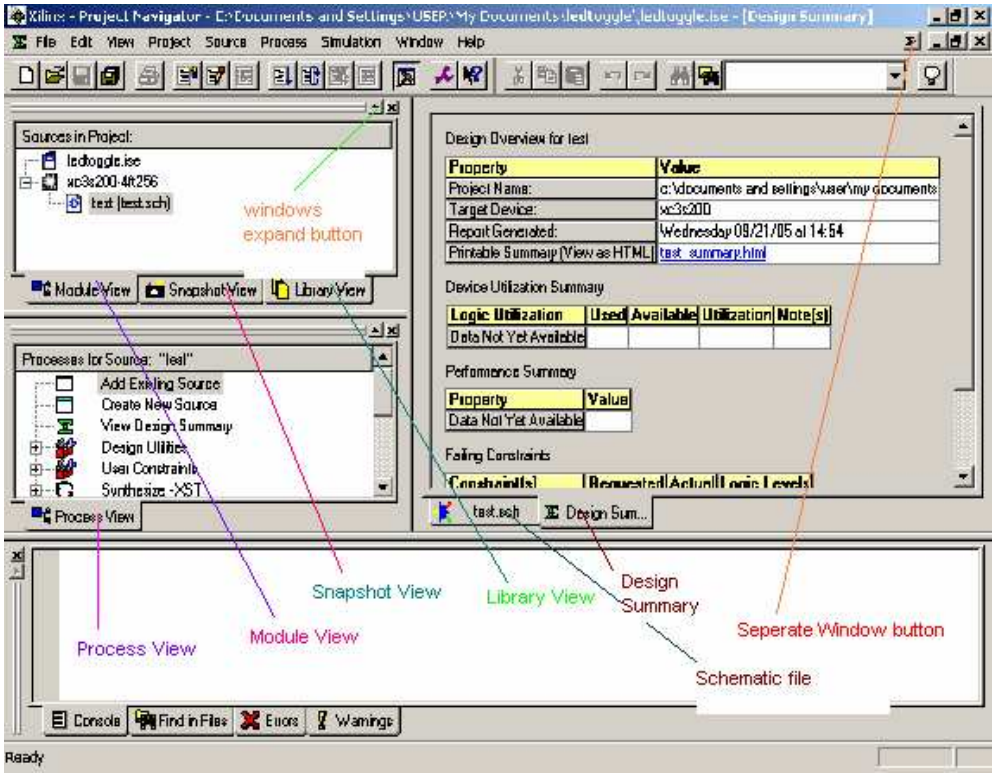
- Click **Next, Next** in the next windows. The final window gives the info about the project click **Finish**



2. Project Navigator Overview:

Project Navigator will be updated with the new project info. The Project Navigator is the interface used to interact with the Xilinx project. There are several Panes that the designer will be using (1) the Sources Pane (upper left side), (2) Processes/Options Pane (middle left side), (3) Working Pane (upper right side, largest area) and (4) the Transcript Pane (lowest pane across the bottom of ProjNav window). Within the panes are tabs that the user will select to perform different tasks. The various tabs that are utilized are highlighted in the next figure The various tabs and buttons are

- *Module View*
- *Snapshot View*
- *Library View*
- *Process view*
- *Schematic File*
- *Design Summary*
- *Windows Expand button*
- *Separate Window button*



a. Sources Pane:
   i. *Module View tab* – hierarchical tree where the structure of the project is provided. This tab is used to open a project files, and select modules for selection of processes.
   ii. *Symbols tab* – tab used to select the various logic components, including modules that the designer creates.

b. Processes/Options Pane:
   i. *Process View tab* – this tab is used to select the various processes that will be performed on the module selected in the Module View tab.

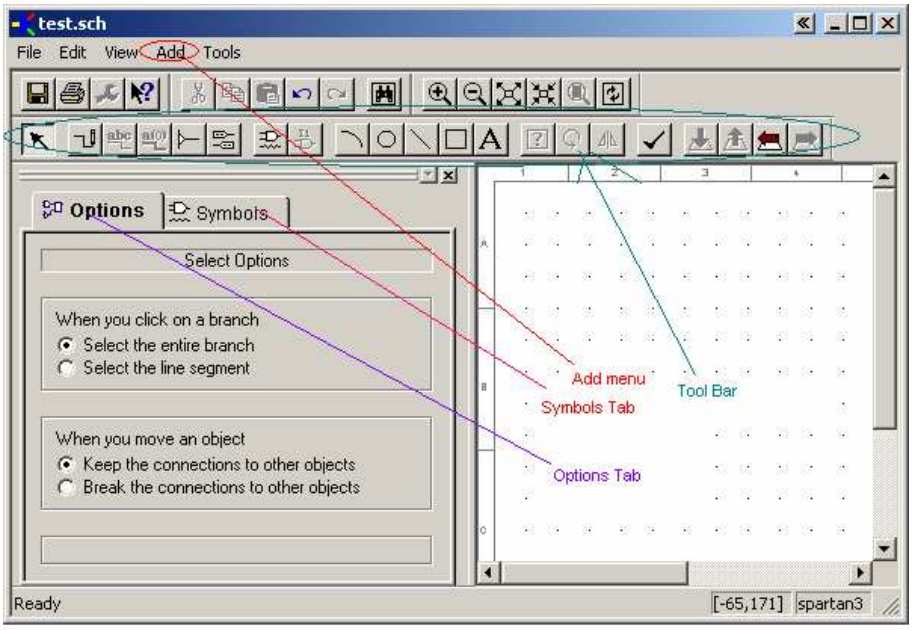
ii. *Options tab* – the options tab is context sensitive. The options present are for the current action being performed. Some of the actions are Selection, Adding Wires (or nets), and renaming Wires (or nets).

c. Working Pane:
This pane contains the current working file (typically Schematic or VHDL/Verilog files). This pane can be disconnected (as performed in the following sections) or can be left attached (or plugged-in to the Project Navigator.)

d. Transcript Pane:
Information about the current process is displayed in the transcript pane. If an error and/or warning is present for the current process they will be abbreviated in the Error and/or Warning tabs in this pane. The Console tab contains the most information about the current process and can be used to get a more concise description of the Warning and/or Error.

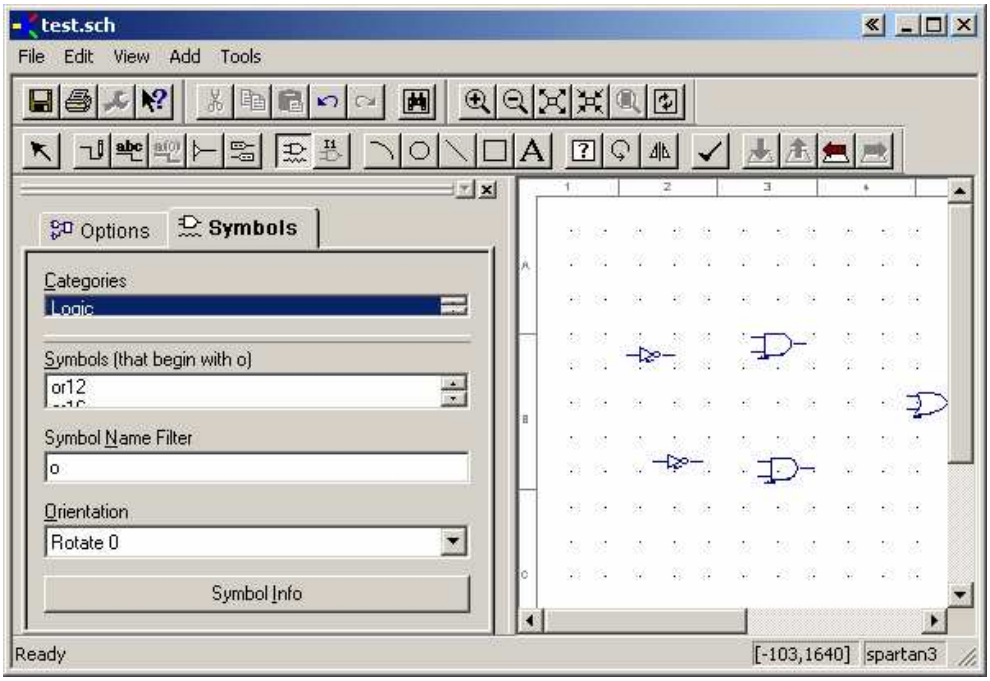
3. Editing a Schematic Source File:

- Use the **Schematic File** tab for working within the schematic page. For current example, schematic file is named **test.sch** click on that or double click on the schematic file name in the *Module View* tab.
- Click on the **Separate Window button** to open the test.sch in a separate window; this step is optional.

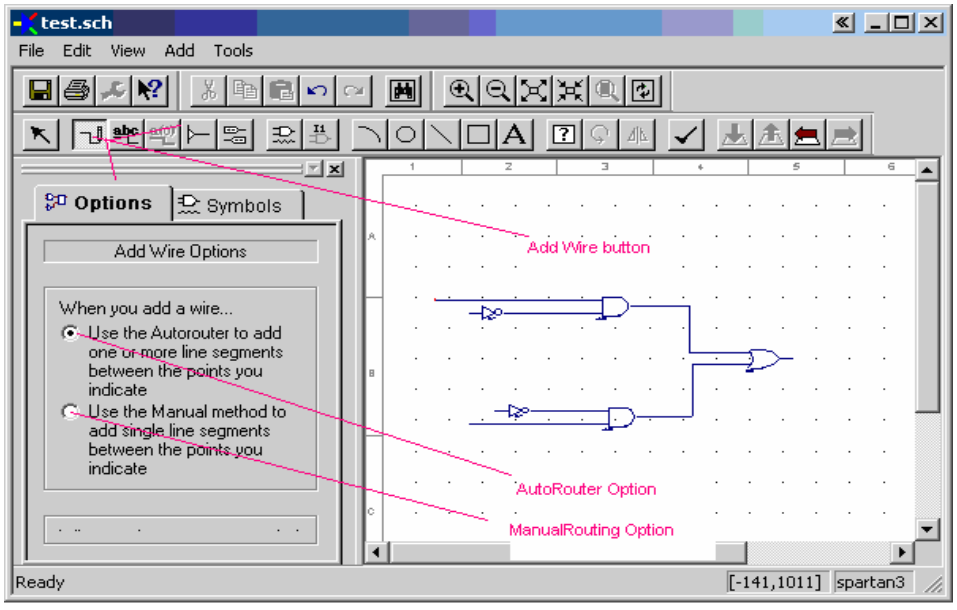


- The **Symbols** tab is used to add gates, encoders, decoders, multiplexers etc.,
- **Add** menu or **Tool Bar** are used to add wires, nets, IO ports (IO Markers) etc.,

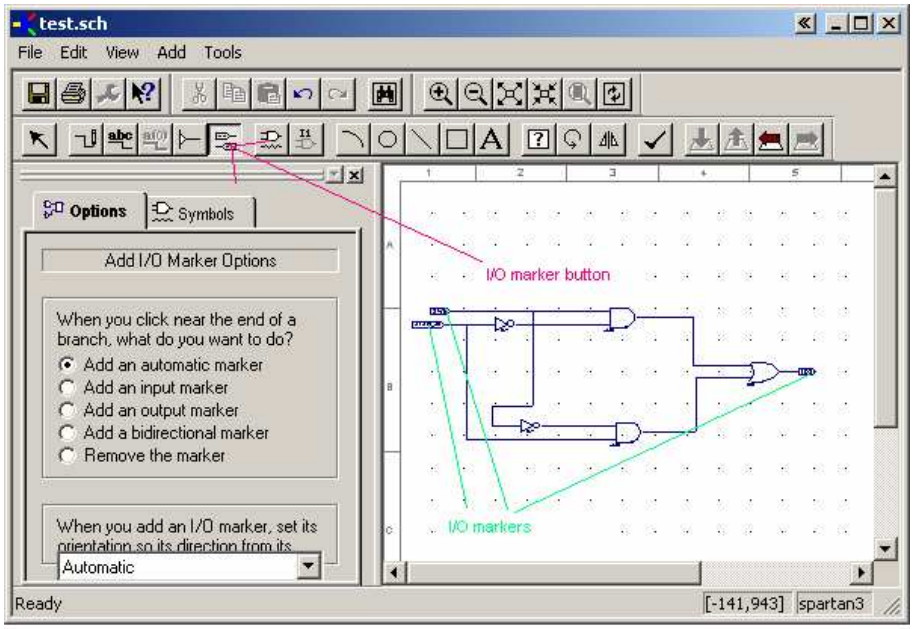
- In the **Symbols** tab, select **Logic** in the **Categories** list box**.** Xilinx primitive models for various logic gates are located in the **Symbols** list box; place two and2, one or2 and two inv gates within the schematic (as shown below). To place a part, select it in the **Symbols** list box and move your mouse cursor to the working schematic, then click on the schematic to place the part, repeat until all the parts are arranged as shown below.



- Click on the Add Wire button in the tool bar (or click on Add menu, then select Wire) to add wires between gates.



- Next add the *I/O Markers* either using the *Add* menu or tool Bar button. IO Markers are the means of connecting the nets to the next level, in this case the next level is the FPGA pins.

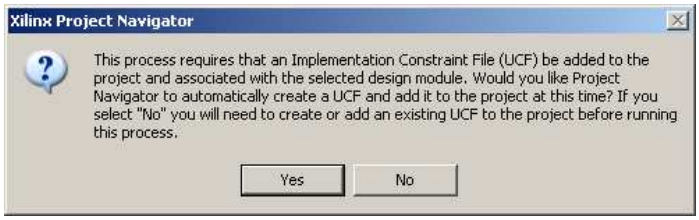


- For this example, SW5, SW6 and LD3 are used as XOR gate inputs and output. The naming of the signals is arbitrary. However, here the designer chose names that coincided with the names on the S3SK board.

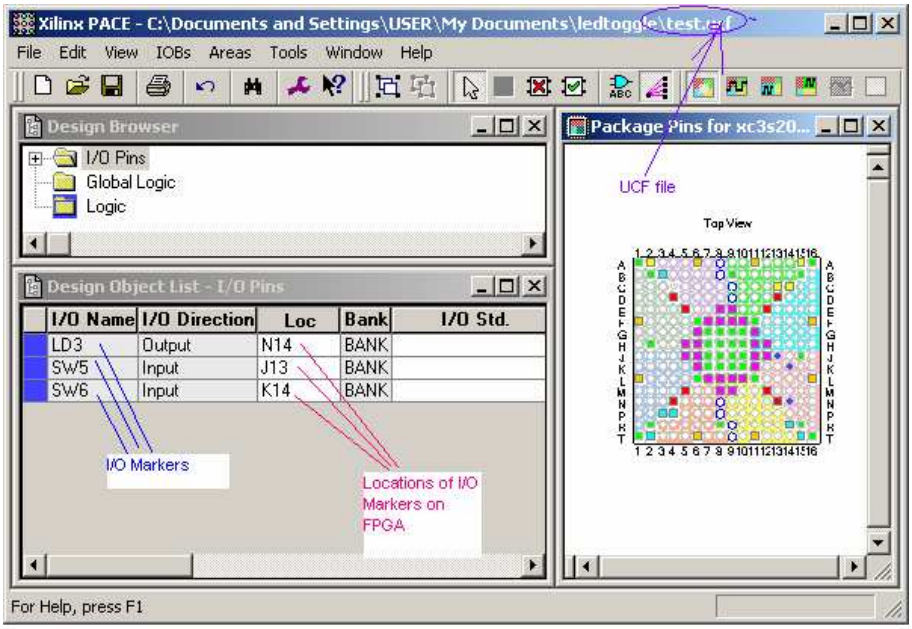
- Now **SAVE** the schematic and return to the Project Navigator window.

4. Assigning FPGA Package Pins to IO Markers:

- With the top-level schematic selected in the Sources/Module View tab, expand **User Constraints** item in the **Process View** tab, then double-click on **Assign Package Pins** and click **Yes** in the following pop-up window.



- UCF file will be opened within Xilinx PACE (a separate program for assigning constraints) as shown below. Now enter the Location of the I/O pins. The Locations or pin numbers are marked on the S3SK board. For this project, SW5, SW6 and LD3 are being used and the corresponding pins are noted on the board as J13, K14, and N14. Insert the respective values in the **Loc** column for the pins to be assigned or simply click on the I/O marker beside I/O Name, drag and drop it in the package view of the FPGA board on the appropriate pin.

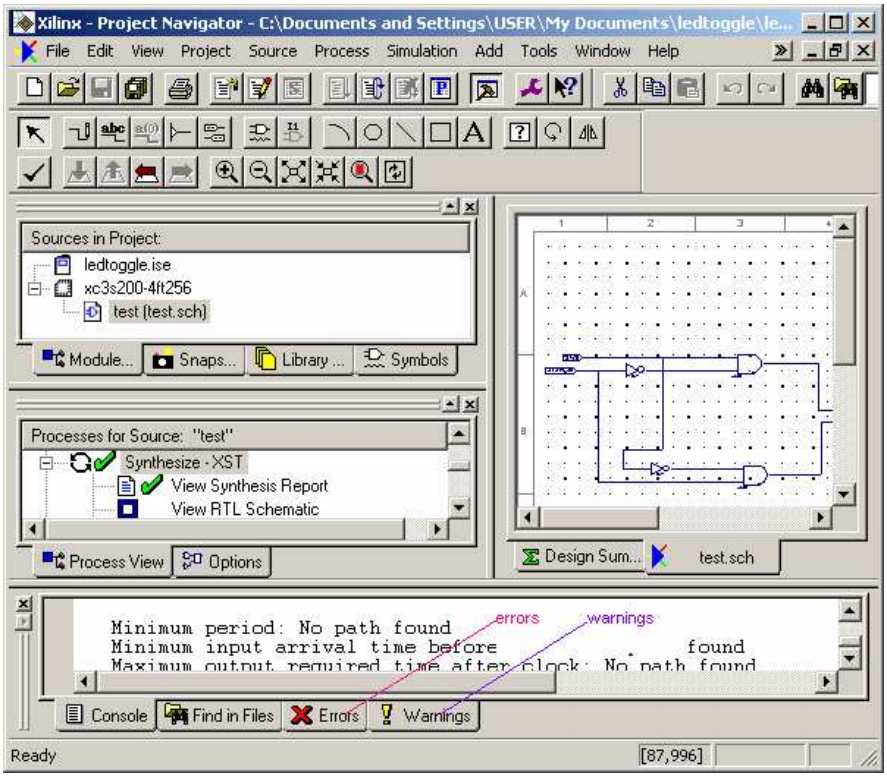


- **Save** the .ucf file and close the Xilinx PACE window.

5. Synthesize the Design:

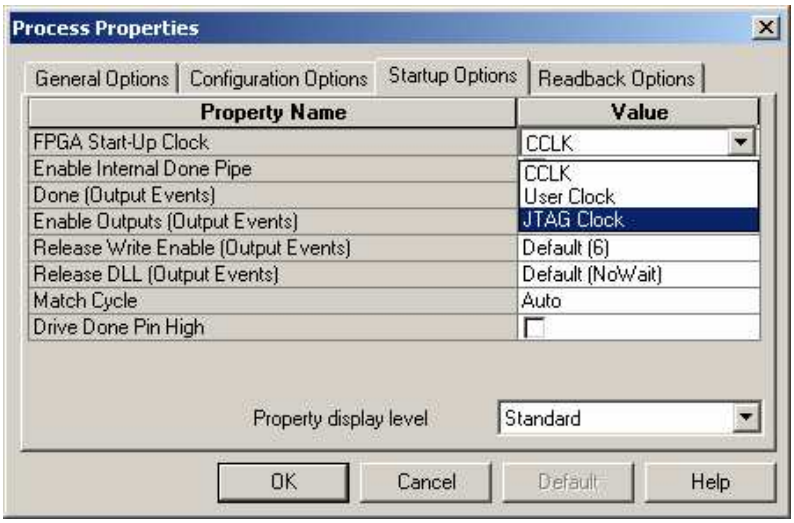
Synthesis is analogous to compiling a computer program, but for hardware. Errors in the design can be captured in this step. If errors/warnings occur then correct them and re-synthesize the design. Repeat this process until no errors and a minimum of warnings are obtained.

- Click on the schematic file (test.sch) in **Module View** tab,
- Click on **Process View** tab,
- Double click on **Synthesize-XST**,
- Wait for the synthesis process to complete, at which point, the **Synthesize-XST** is checked (in green) which means the schematic file is synthesizable. If it is not synthesizable a yellow exclamation point or a red X will appear next to **Synthesize-XST** in the **Processes Pane**, in which case, you have to check for warnings and/or errors and correct them and redo the synthesis until all errors are gone.



6. Generate Programming File (.bit file)

- Right click on **Generate Programming File** in **Process View** tab,
- Click on **properties**,
- Click on **Startup Options** tab,
- Select **JTAG clock** in the drop-down menu of **FPGA start-up clock**,
- Then click **OK**.

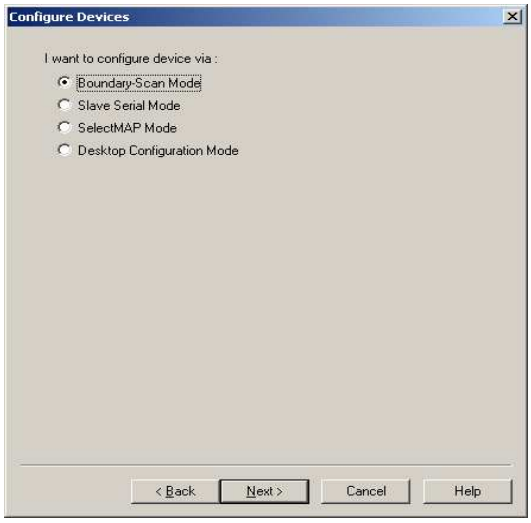


- Next, double click on **Generate Programming File** and wait until the **Implement Design** and Generate **Programming File** are checked in green, again if they are not checked, check for errors and warnings as explained above and repeat this step.

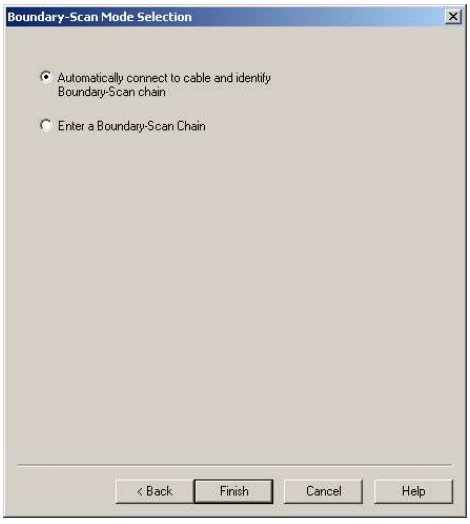
7. Configuring the FPGA:

Configuring the FPGA consists of downloading the .bit file to the FPGA. Once power is lost then restored the FPGA will be configured from the EEPROM IC located on the S3SK board. For this class, the student will not need to download the code to the EEPROM. Thus, the steps for programming the EEPROM are not included here.

- Start by expand the **Generate Programming File** item in the processes view and double-click on **Configure Device (iMPACT)**,
- On the **Configure Devices** dialog box that appears, ensure **Boundary Scan Mode** is selected.

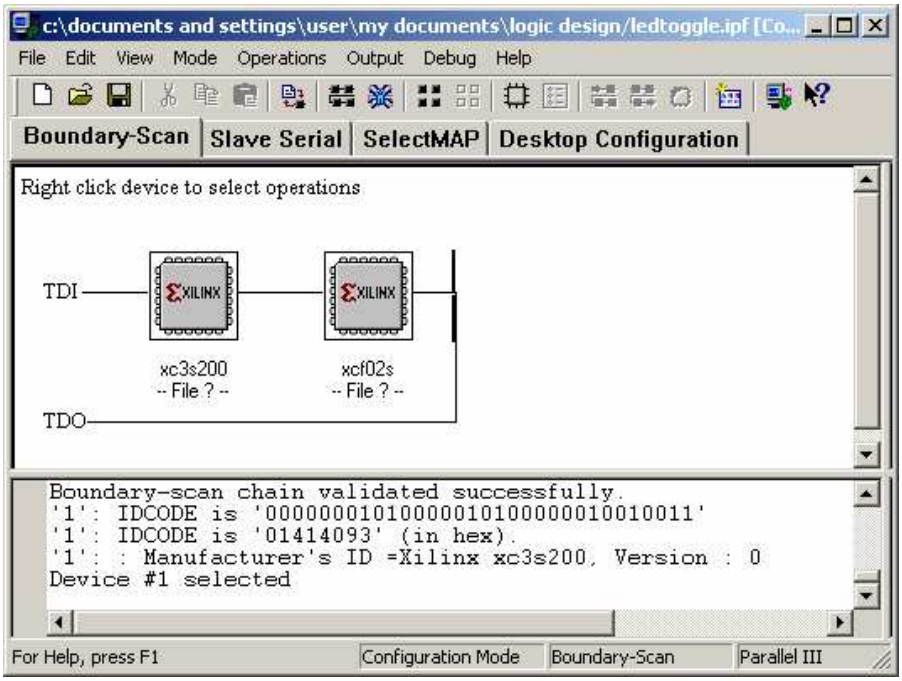


- Click **Next**, select **Automatically connect to cable and identify Boundary Scan** chain and then click **Finish**



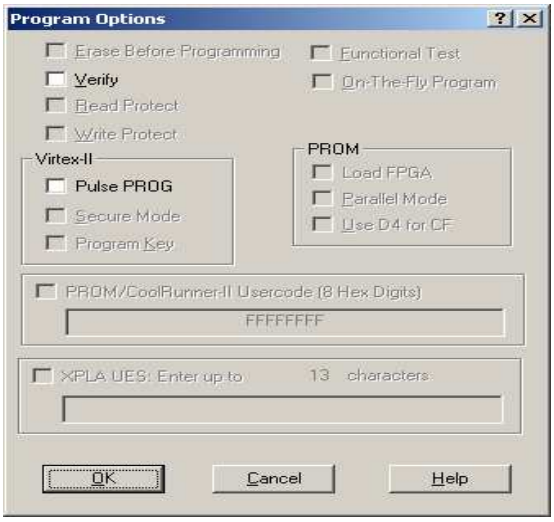
- Then, click **OK** in the **Boundary-Scan Chain Contents Summary** dialog box.

The following application window (iMPACT) will appear.

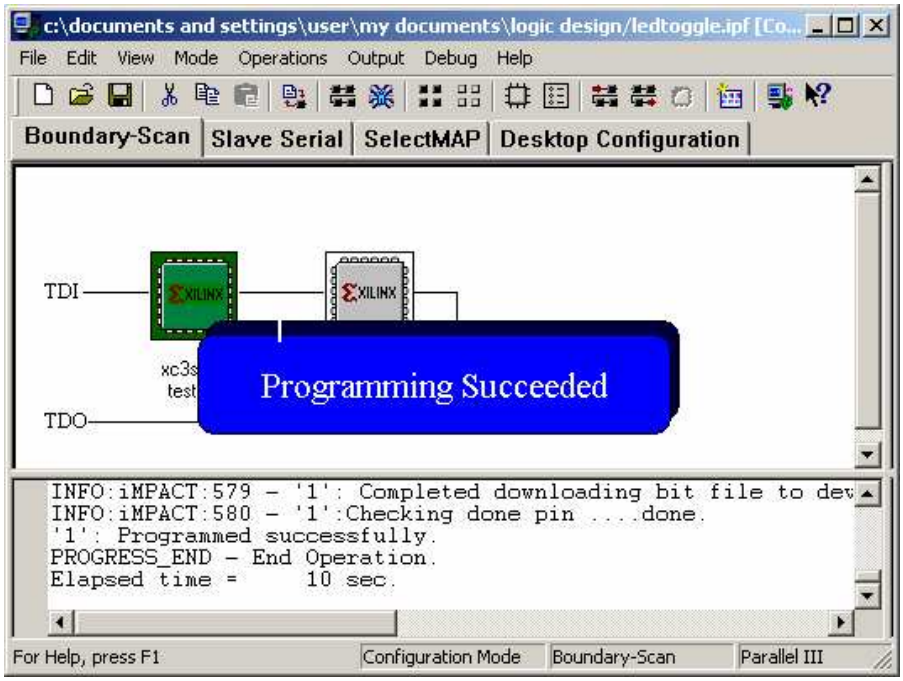


- The first IC in the chain is the FPGA and second is the EPROM. Double –click on the **xc3s200** IC to assign the configuration file and select the bit file *(test.bit)* and click **open**.

- Now, right-click on the **xc3s200** and then click **program** and click **OK**



- Then, the bit file will be downloaded onto FPGA



- *Testing:* Now we can check the XOR gate operation using the slider switches SW6 and SW5 as inputs and LED (LD3) to observe the output. When one of the switches is high the LED should be on and otherwise LED should be OFF.

8. Finishing Up:

- Close the **iMPACT** application, you will be asked to save your work; select **Yes**.
- Close the **Project Navigator** application; if you have not done so you will be asked to save any or all files, select **Yes**.

The project can be downloaded to the S3SK board at a later date by starting the iMPACT application from the Windows Start Menu, then right clicking on the FPGA in the boundary-scan chain and assigning the appropriate .bit file.

APPENDIX

Creating a Module (or model) Using Schematic Entry

Schematics can be used to create a model (or module) for use in other schematics. This is desired when the same block is to be repeated several times or for making the design more readable. When the designer creates modules to be used within other schematics, it is referred to as a hierarchical design. Whether the student realizes it or not this has already happened. The AND, OR and INV gates used in this document are primitive models with a symbol file attached. The following steps should be used to make a schematic sheet into a model with a symbol file associated to it:

- Create a new schematic with the functionality desired,
- Ensure that all I/O signals for the model have IO Markers attached,
- Save schematic sheet to be converted,
- Create a symbol for that sheet,
- Go to the schematic sheet that will receive the new module and
- Place the new module in the upper level schematics.

1. Creating a new schematic sheet:
    a. Right-click on a module in the current project,
    b. Select New Source,
        i. Make the new source a schematic,
        ii. Ensure that it will reside in the current project directory (this is a default setting),
        iii. Click Finish, and the new sheet appears. It will show up as a new module in the Sources window with the same level as the top-level schematic.
    c. Enter the desired functionality in the schematic sheet,
    d. All signals that are required external to the module should contain IO Markers.
    e. Save the file.

2. Creating a symbol from a schematic
    a. Select the schematic that will have a symbol created in the Sources Pane,
    b. Make the Process View tab visible,
    c. Expand Design Utilities option under in the Process Pane, and
    d. Select Create Schematic Symbol.
        i. If no errors were found then the symbol is now created within the project directory,
        ii. Else, correct errors and retry.
    e. The module is now ready to be used in this or any other project.
        To use the new module and symbol, the .sch and the .sym files must be placed in the new project directory.

3. Placing the symbol a higher level schematic sheet
    a. Select the schematic sheet to receive the new module in the Working Pane,
    b. Select the Symbols tab,
    c. Under Categories in the Sources Pane, select the project directory,
    d. Click on the new module, and
    e. Place the symbol in the upper level schematic sheet.

4. Once the part is placed and all files are saved for the project the new module will appear under the sheet where the module was placed.

NOTE: if the module that you want to use in a design resides in another directory (i.e., a library directory), then right click on any module in the sources pane and select Add Copy of Source option. Browse to the location of the module and select it. Both the symbol and the schematic sheet will be copied to the current project directory.