UNC Charlotte, Department of Electrical and Computer Engineering
ECGR 2181, Fall 2008, Homework #6
Due: 11/5/2008, at the beginning of class (100 points)

Show all of your work!!!!!

1. How long did this assignment take you? (Answer truthfully!) (5 points)
2. Write the VHDL statements that represent the prime number detector with a behavioral model for all prime numbers between 0 and 63. Assume a bus with input "i", six bits wide and a circuit enable bit "en_L" (enable, active low); also assume output "F", one bit wide.

   You will need to write ALL of the statements that would allow this file to be synthesized in our Xillinx tools. (95 points)