UNC Charlotte, Department of Electrical and Computer Engineering
ECGR 2181, Fall 2008, Homework #9
Due: 12/1/2008, at the beginning of class (100 points)

Show all of your work!!!!!

1. How long did this assignment take you? (Answer truthfully!) (5 points)
2. Consider the second problem from Homework Assignment #8:
   Draw a state diagram for a Finite State Machine with one input, *z*, and three outputs, *a, b, c*. *abc* should always follow the following sequence when $z = 0$: 000, 001, 011, 111, 101, 100, 110, 010, repeat. *abc* should go to the previous value (i.e. 011 to 001) when $z=1$. The output should only change on a rising clock edge. Make 000 the initial state.

   Implement this FSM in VHDL. Turn in the TYPED VHDL code (hint – you can check your work if you simulate it). (95 points)