

UNCC – ECGR2181- Midterm Exam 2 – November 11, 2008

C

Name: Solutions

Mosaic User ID _____

Question	1-10	11	12	13	14	15	16	17	Total
Score	39/35	10/10	15/15	20/20	20/20	20/20	20/20	10/10	150/150

You are permitted 75 minutes to take this test, no more. You are allowed the following items for the test: single sheet of paper with notes, pencils and erasers. You are not permitted to have any of the following on your desk during the test: calculator, books, notes, homework, labs computer, cell phone, or other electronic assistance. Failure to abide by this policy will result in a zero for the test and a visit to the UNC Charlotte honor board. Put your answers on paper provided, and turn in this sheet and the answer pages - use only that paper.

Please read and sign this statement: I have not received from anyone nor assisted others while taking this test. I have also notified the test proctor of any of these violations noted above.

Signature: Solutions

For these multiple choice and True/False problems, circle the SINGLE best answer (letter and answer) for each problem. *All or nothing for each*

- How many levels of 4 input mux are needed for a 64 input mux? (5 points)
 - a. 1
 - b. 2
 - c. 3
 - d. 4
 - e. None of these
- In which of the following cases has overflow not occurred (two-complement number)? (5 points)
 - a. The MSB of first number is 0 and of second number is 0 and MSB of the result is 1.
 - b. The MSB of first number is 1 and of second number is 0 and MSB of the result is 1.
 - c. The MSB of first number is 1 and of second number is 1 and MSB of the result is 0.
 - d. Carry into the MSB is 1 and carry out of the MSB bit is 0.
 - e. None of the above.
- Oscillation in the output Q can occur when the input to the SR latch is (5 points):
 - a. S = 1, R = 1
 - b. S = 1, R = 0
 - c. S = 0, R = 0
 - d. S = 0, R = 1
- Which of the following statements is false (5 points):
 - a. All microprocessors have some form of an ALU
 - b. If the carry into the sign bit differs from the carry out of that column, it implies an overflow has occurred in the addition
 - c. A suitable combination of only AND gates is sufficient to construct an adder/subtractor
 - d. A 4-bit equality comparator outputs 1 if two 4-bit numbers are equal
 - e. All of these statements is true.
- Write the function for Full adder where inputs 'a' and 'b' are the numbers added, and input 'c' is the carry-in. Also, 's' and 'co' are sum and carry out, respectively (5 points):
 - a. $co = bc + ac + ab$ $s = a \text{ xor } b \text{ xor } c$
 - b. $co = b'c + ac + ab$ $s = a \text{ xor } b \text{ xor } c$
 - c. $co = bc + ac + ab'$ $s = a \text{ xor } b \text{ xor } c$
 - d. $co = b'c + ac' + ab'$ $s = a \text{ xor } b \text{ xor } c$
- All VHDL statements are executed in sequential order.

TRUE FALSE (2 points)
- A multiplexer routes a single input to one of several outputs, based on the value of the select lines.

TRUE FALSE (2 points)

8. A decoder with an enable input can be used as a substitute for a demultiplexer.
 TRUE FALSE (2 points)
9. A Full Adder can always be used in the place of Half Adder, provided you assign the correct value to C-in.
 TRUE FALSE (2 points)
10. A VHDL component is a predefined description of a logic function that can be used in multiple times in a design.
 TRUE FALSE (2 points)
11. Consider the following clock signal:

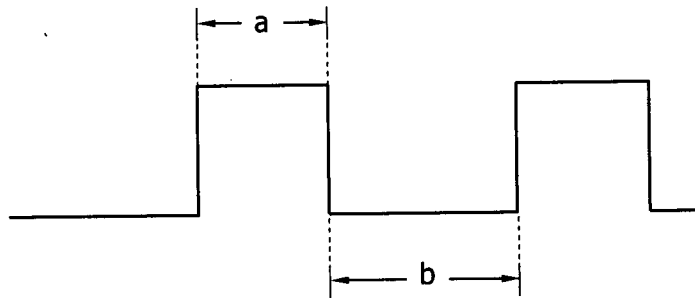


Figure 1, Clock Signal

- a. (5 pts.) Give the equation for duty cycle (%) of the waveform in Figure 1, where a and b have units of time.

duty cycle % = $\frac{a}{a+b} \times 100$ 1pt trying
 3pts formula, without 100
 1pt 100%

- b. (3 pts.) Assume the waveform is cyclic. Express the frequency of the clock in terms of a & b.

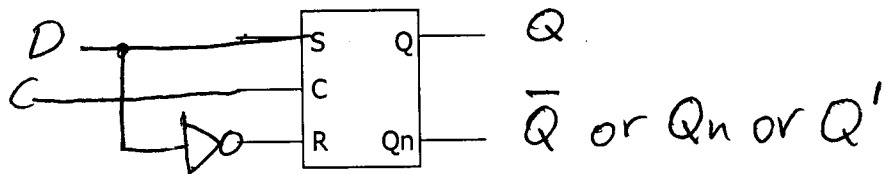
$f = \frac{1}{a+b}$ 3pts, all or nothing

- c. (2 pts.) The time between falling edge and rising edge is given by _____
 a or b (circle one)

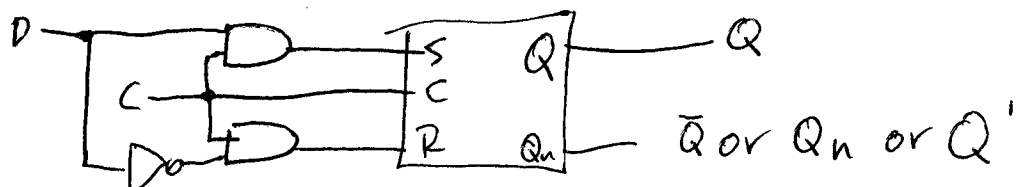
2pts, all or nothing

12. (15 pts.) Convert a SR Latch w/ enable into a D - Latch. Use the following symbol and any ordinary gates necessary to complete the task.

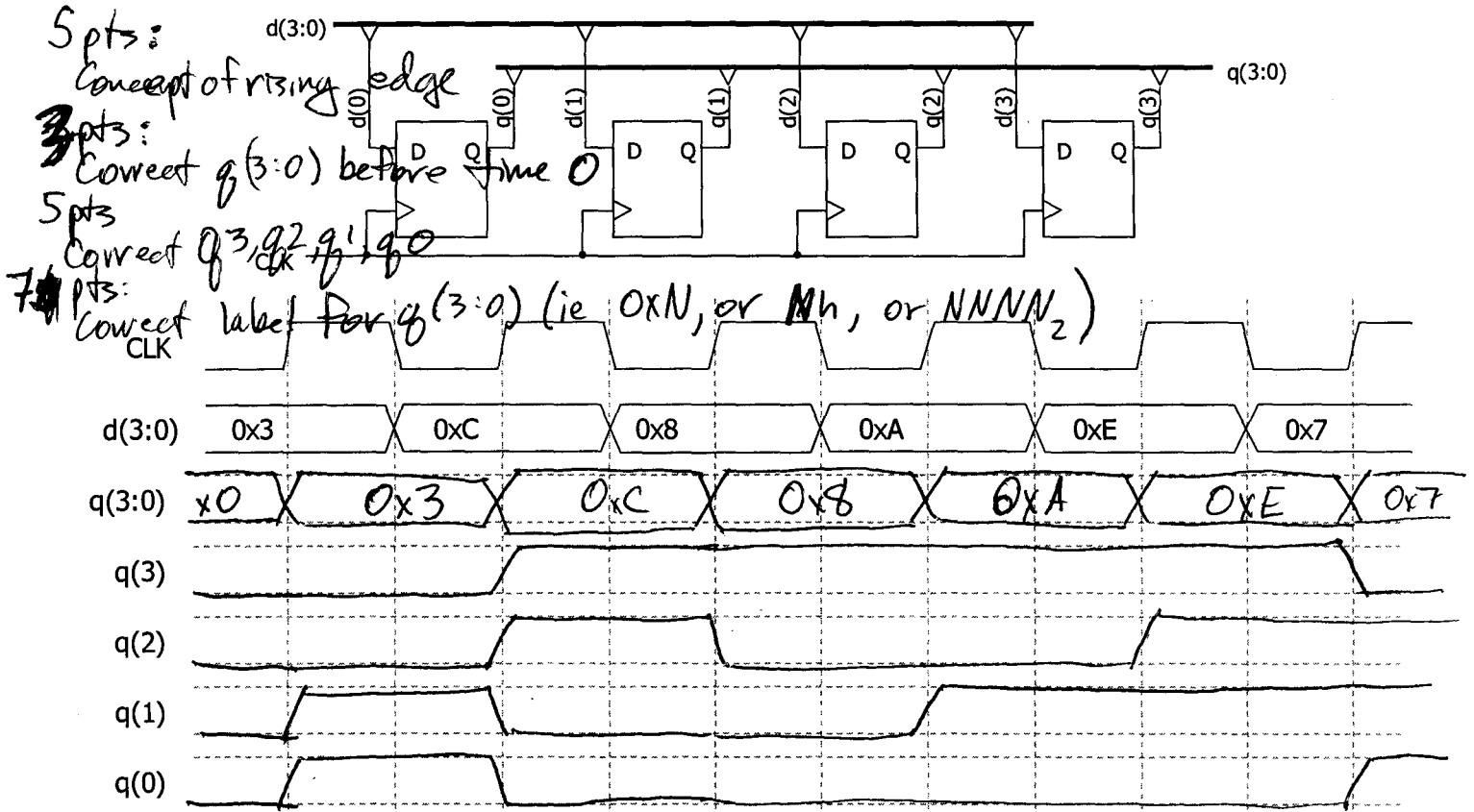
5pts: only not gate (2 points if design below)
 5pts: label inputs/outputs
 5pts: for trying



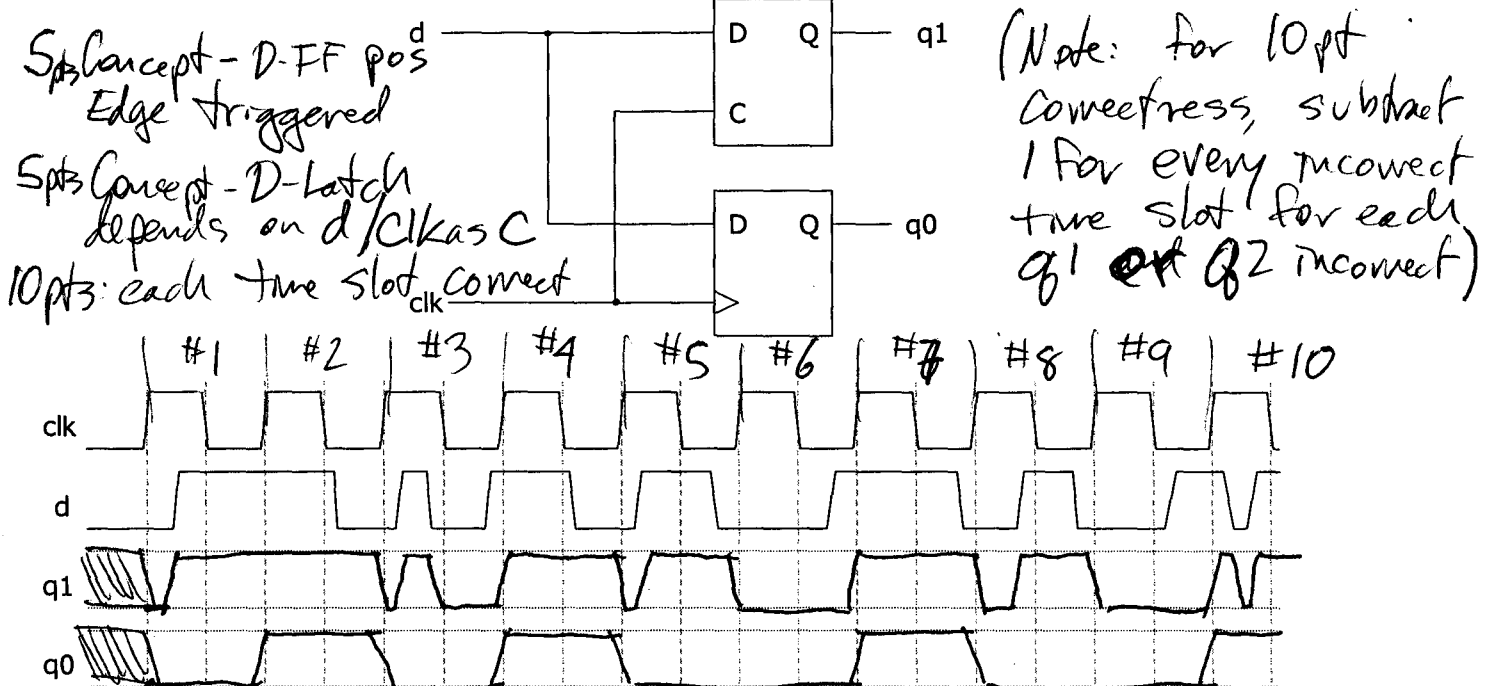
Note
 -3 for this



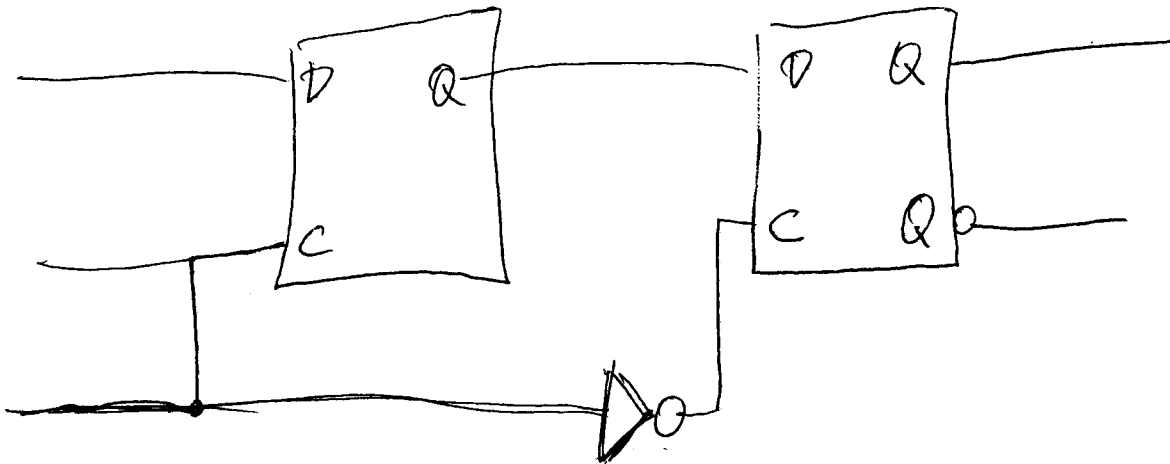
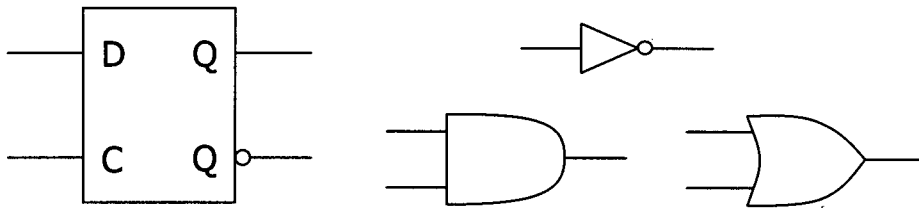
13. (20 pts.) Determine the output bus values for the circuit and functional timing diagram given below. (Functional timing diagrams assume $t_p = 0$ s.) $q(3:0)$ is logic '0' at $t=0$ ns.



14. (20 pts.) Based on the logic diagram given complete the functional timing diagram in the space provided.



15. (20 pts.) Draw the circuit that makes up the Falling-Edge triggered, D Flip-flop using only the parts shown below. Circle the input and output labels. Use each part as many times as necessary and it is not necessary to use all the parts.



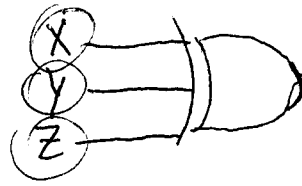
Spts Concept that a FF needs 2 Latches
 Spts Not gate
 Spts Not gate on the correct latch
 Spts Trying

16. (20 points) Consider three one-bit numbers, x, y, and z. Create an adder circuit using only gates that adds these three bits together and outputs them as s1 and s0 (s1 is the most significant bit). We do not have any carry bits. *This is simply an adder!*

(abc _{in})	Carry S
x y z	s ₁ s ₀
0 0 0	0 0
0 0 1	0 1
0 1 0	0 1
0 1 1	1 0
1 0 0	0 1
1 0 1	1 0
1 1 0	1 0
1 1 1	1 1

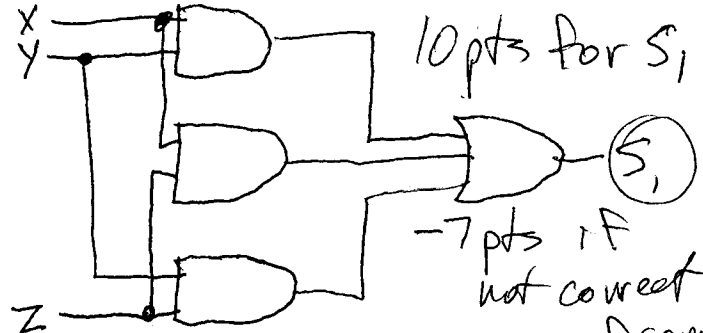
$$s_1 = xy + yz + xz$$

$$s_0 = x \oplus y \oplus z$$



10 pts for s₀

-7 pts if not correct
-3 pts if not optimal



10 pts for s₁

-7 pts if not correct
-3 pts if correct but not optimal

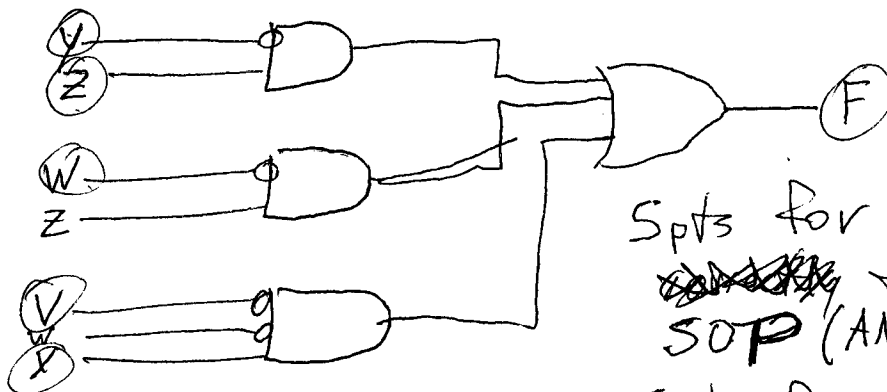
17. (10 points) Consider the following VHDL Code. Draw an equivalent schematic of the circuit using only logic gates.

```
library IEEE;
use IEEE.std_logic_1164.all;
```

```
entity fewgates is port
  (V, W, X, Y, Z: in std_logic;
   F: out std_logic );
end fewgates;
```

```
Architecture behavioral of fewgates is
begin
  process (V, W, X, Y, Z) begin
    F <= ((NOT Y) AND Z) OR ((NOT W) AND Z) OR ((NOT V) AND (NOT W) AND X);
  end process;
end behavioral;
```

$$F = y'z + w'z + v'w'x$$



5 pts for converting ~~to~~ to two level SOP (AND/OR)

5 pts for correct input & connection