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UNCC – ECGR2181- Midterm Exam 1 – October 1, 2008

Name: Solutions **Mosaic User ID** _____

Question	1-13	14	15	16	17	18	19	Total
Score	/50	/10	/10	/20	/20	/20	/20	/150

You are permitted 75 minutes to take this test, no more. You are allowed the following items for the test: single sheet of paper with notes, pencils and erasers. You are not permitted to have any of the following on your desk during the test: calculator, books, notes, homework, labs computer, cell phone, or other electronic assistance. Failure to abide by this policy will result in a zero for the test and a visit to the UNC Charlotte honor board. Put your answers on paper provided, and turn in this sheet and the answer pages - use only that paper.

Please read and sign this statement: I have not received from anyone nor assisted others while taking this test. I have also notified the test proctor of any of these violations noted above.

Signature: Solutions

For these multiple choice and True/False problems, circle the SINGLE best answer (letter and answer) for each problem. All or None

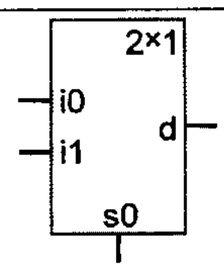
1. The ASCII ~~string~~ "49ER" is represented by the values 0x52576982
   TRUE (FALSE) (2 points)
   This is the decimal value for the string
2. VHDL, Verilog, and Xillinx are all examples of hardware description languages used to synthesize digital circuits?
   TRUE (FALSE) (2 points)
3. ~~Any~~ Boolean function can be implemented using just NAND gates.
   (TRUE) FALSE (2 points)
4. The operation of adding the 8-bit 2's complement number 0x7F to the 8-bit 2's complement number 0xD0 and storing the result in a the 8-bit 2's complement number will result in overflow.
   TRUE (FALSE) (2 points)
   Positive + Negative can never be Overflow
5. The sign extension of the 8-bit 2's complement number 0x80 to a 16-bit 2's complement number is 0x8000.
   TRUE (FALSE) (2 points)
   would be 0xFF80

6. What type of circuit is characterized by only active components with no memory? (5 points)
   a. Sequential
   (b. Combinational)
   c. Holistic
   d. Schematic
   e. None of the above

7. What is the name of the device at the right? (5 points)
   (a. NOR)
   b. NAND
   c. XOR
   d. Decoder
   e. None of the above

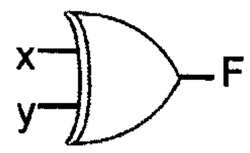
8. What is the name of the device at the right? (5 points)

a. XOR
c. MUX
e. None of the above
b. Encoder
d. Decoder



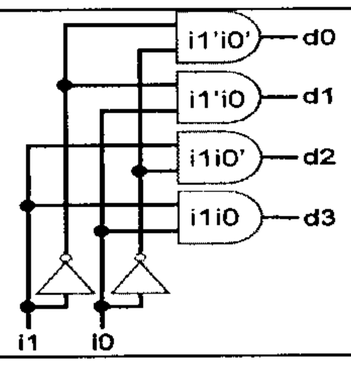
9. What is the name of the device at the right? (5 points)

a. NOR
c. XOR
e. None of the above
b. Encoder
d. Decoder



10. What is the name of the device at the right? (5 points)

a. XOR
c. MUX
e. None of the above
b. Encoder
d. Decoder



11. Which of the following is not a Boolean algebra property? (5 points)

a. a + b = b + a
b. a + (b * c) = (a + b) * (a + c)
c. 1 * a = a * 1 = a
d. (ab)' = a' + b'
e. a + a = a
f. All of these are valid properties

12. Which of the following is not an example of an Embedded System? (5 points)

a. Automobile
b. Mobile Phone
c. Dell Laptop PC
d. An HP Laser Printer
e. An electronic keyboard

13. Given a digital system with 6 inputs, how many different variations are there for those 6 inputs? (5 points)

a. 6
d. -32 to +31
b. 36
e. None of the above
c. 64

14. Convert the following. Circle your final answer.

a. The unsigned byte 76_{10} to hexadecimal (5 points)

$76 - 64 = 12 - 8 = 4 - 4$

$2^6 \quad 2^3 \quad 2^2$

7 6 5 4 3 2 1 0
0 1 0 0 1 1 0 0
4 C

4Ch or 0x4C or $4C_{16}$

b. The signed byte 0xD4 to decimal (5 points)

(*Note: assume signed byte is a 2's complement 8-bit value)

11010100_2 (-128 64 16 4 2 1)

$64 + 20 = 84$

$-128 + 84 = -44$

or

$00101100 = 44$ (32 8 4)

-44_{10}

15. Give the minterm list for the following truth table: (10 points)

x	y	z	F	
0	0	0	1	0
0	0	1	0	1
0	1	0	0	2
0	1	1	0	3
1	0	0	1	4
1	0	1	1	5
1	1	0	0	6
1	1	1	1	7

$F(x,y,z) = \Sigma m(0,4,5,7)$

-4 pts for not including (x,y,z) or wrong order

-4 pts for being shifted by one (i.e.) (1,5,6,8)

16. Using **Boolean algebra** reduce the following expression to a system description that would use the least amount of area on an integrated circuit (assume CMOS transistors are used). Of primary importance is the speed (i.e., make the final equation represent a two level circuit (SOP)). (20 points)

$$F(a,b,c,d) = ((a+b'+d')\cdot(c+d)\cdot(a'+c+d)\cdot(a+b+d'))'$$

$F(a,b,c,d) = (a+b'+d')' + (c+d)' + (a'+c+d)' + (a+b+d')'$

$= a'bd + c'd' + ac'd' + a'b'd$

$= a'd(b+b') + c'd'(1+a)$

$b+b'=1$ $\qquad$ $1+a=1$

$= a'd \cdot 1 + c'd' \cdot 1$

$$\boxed{F(a,b,c,d) = a'd + c'd'}$$

**Small Mistakes (dropped or added inversion)

1 - -2 pts

2 - -2 pts

3 - -2 pts

4 or more well this counts as big mistake

*Boolean Algebraic mistake ~~pts each~~

*5 pts each.

* not to exceed -18 pts if student ~~tries~~ makes good attempt; or -20 pts. if no attempt.

17. Implement a 3-input XOR gate using only a 4x1 multiplexer and an inverter. Also complete the truth table with the correct labels and function solution. Fully label all inputs and outputs. (20 points)

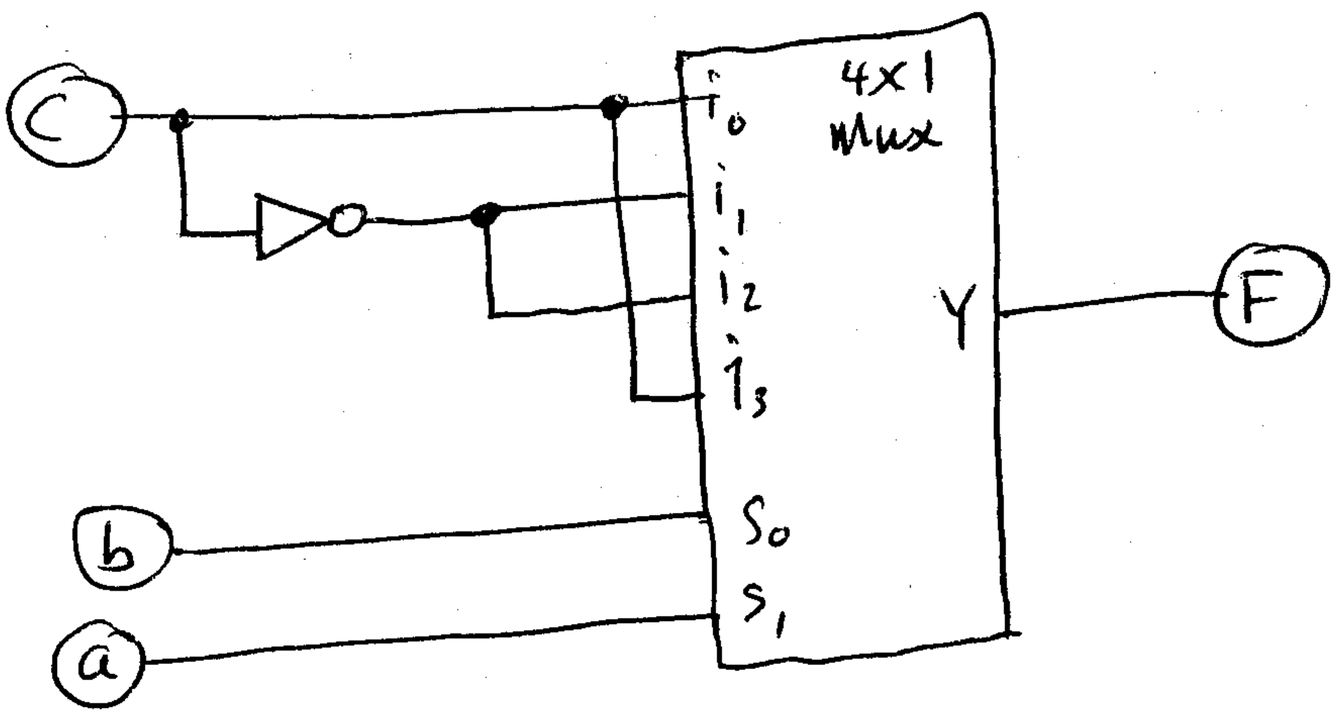
a	b	c	$F = a \oplus b \oplus c$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$i_0 = c$

$i_1 = c'$

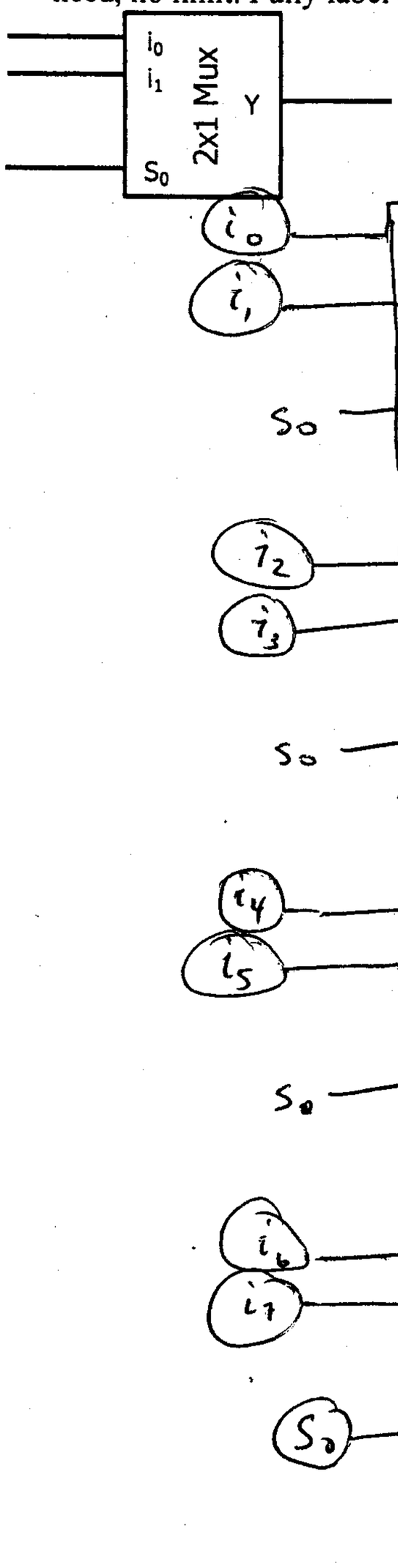
$i_2 = c'$

$i_3 = c$



* missing connection Dots - 2 pts
* I/o not properly labeled - 2 pts
* correct T.T. - [redacted] - 8 pts
* mux configuration from T.T. — 8 pts — note: Correctness of T.T. should not effect this score

18. Design an 8x1 multiplexer using only 2x1 multiplexers (shown below.) Use as many of the 2x1 muxes as you need, no limit. Fully label all inputs and outputs. (20 points)



+ proper labels — −2 pts
~~* disallowed Components −2 pts/instance max 5 instances~~
+ ~~if~~ on the disallowed Components but works −8 pts
* disallowed components, does not work −10 pts discretionary
* only muxes but does not work − 16 pts discretionary

19. Design a logic circuit using the following truth table. Use only basic logic gates (AND, OR, Inv.). Also, the circuit should use the fewest number of gates and the fewest number of inputs to the gates. Fully label all inputs and outputs. (20 points)

a	b	c	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

~~a'b'c'd'~~

a'b'c' + a'bc' + ab'c' + ab'c

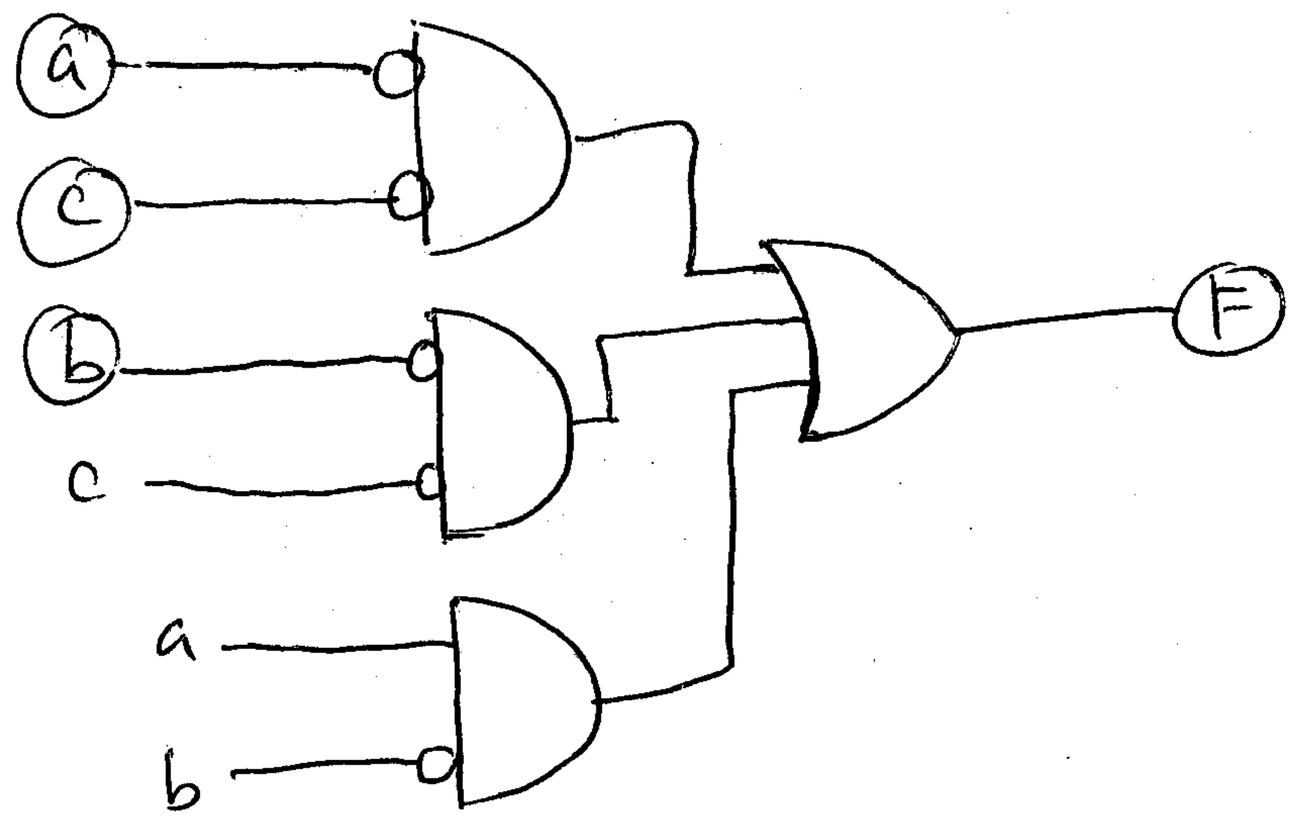
① ② ③ ④

1 & 2: a'c'

3 & 4: ab'

F(a,b,c) = a'c' + ~~bc~~ + ab'

+10 pts correct Equation



+10 pts correct circuit from equation (independent of equation Correctness)

* gates must clearly be AND or & OR & / or Inverters
* bubbles can be inverters