Computer Assignment 1

ECGR 2181 - Fall 2009

Assignment Overview

In this assignment you will use Xilinx ISE 7.1i and ModelSim to build and simulate designs created from schematics. The assignment is broken into two sections, **Decoders** and **Multiplexers** (muxes). Using the techniques learned from the CAD Tutorial complete both sections and demo the final simulations to one of the TAs during their Office Hours (in Woodward 200). In addition you will need to turn in the printed schematics listed below along with the Grade Rubric.

The Computer Assignment is due Wednesday, October 28th by 3 PM.

Getting Started

1. Create a new directory to store all of the Computer Assignment Files
2. Open **Xilinx ISE 7.1i** and Create a New Project in the newly created direction called: **computer_assignment_1**
3. Create it for the **Nexys2 Board** (Spartan 3E, xc3s500e, fg320, -4)
4. Add 1 New Source File called of type Schematic: **dec_2_to_4_sch**
5. Click Next / Finish to complete the New Project Wizard
6. Add the following Source Files of type Schematic to the Project:
    a. dec_4_to_16_sch
    b. mux_4_to_1_sch
    c. mux_16_to_1_sch

Decoder

1. **2 to 4 Decoder** (dec_2_to_4_sch)
    a. Create a schematic of a 2 to 4 Decoder from Gates (AND, OR, NOT)
    b. Inputs: i0, i1, enable
    c. Outputs: d0, d1, d2, d3
2. **4 to 16 Decoder** (dec_4_to_16_sch)
    a. Create a schematic of a 4 to 16 Decoder from multiple 2 to 4 Decoders that was created above (not the decoder that already exists in the component library).
    b. Inputs: i(3:0), enable
        i. Input i(3:0) is a 4-bit vector consisting of: i(0) = i0, i(1) = i1, i(2) = i2, i(3) = i3
    c. Outputs: d0, d1, d2, d3, d4… d15
3. **Simulation of 4 to 16 Decoder**
    a. Add a New Source of type Test Bench Waveform called: **dec_4_to_16_tb**
        i. Set the Clock Information to: Combinatorial (or internal clock)
        ii. Set the Initial Length of Test Bench to: 2000 ns
        iii. Set the i(3:0) input to Count Up for 16 Cycles
        iv. Set the Enable Bit to ‘1’ from Time 0 ns to 1600 ns then set the Enable Bit to ‘0’
        v. Save and Simulate Behavioral Model to verify correct functionality
        * See Page 4 of this Handout for the Expected Waveform Output
4. Print out the Schematic of the 2 to 4 Decoder
5. Print out the Schematic of the 4 to 16 Decoder

Multiplexers

1. **4 to 1 Multiplexer** (mux_4_to_1_sch)
    a. Create a 4 to 1 Multiplexer from Gates (AND, OR, NOT)
    b. Inputs: i0, i1, i2, i3, s0, s1
    c. Output: f
2. **16 to 1 Multiplexer** (mux_16_to_1_sch)
    a. Create a 16 to 1 Multiplexer from multiple 4 to 1 Multiplexers that was created above (not the multiplexer that already exists in the component library).
    b. Inputs: i0, i1, i2… i15, s(3:0)
        i. Select s(3:0) is a 4-bit vector where s(0) = s0, s(1) = s1, s(2) = s2, s(3) = s3
    c. Output: f
3. **Simulation of 16 to 1 Multiplexer**
    a. Add a New Source of Type Test Bench Waveform called: mux_16_to_1_tb
        i. Set the Clock Information to: Combinatorial (or internal clock)
        ii. Set the Initial Length of Test Bench to: 2000 ns
        iii. Set the s(3:0) input to Count Up for 16 Cycles
        iv. Set each Input (i0, i1, i2…etc) to be '1' for 1 Clock Cycle
            1. Set i0 = '1' from 0 ns to 100 ns (set to '0' for remainder of time)
            2. Set i1 = '1' from 100 ns to 200 ns (set to '0' for remainder of time)
            3. Set i2 = '1' from 200 ns to 300 ns (set to '0' for remainder of time)
            4. Repeat so that each Input is '1' for 100 ns after the previous input
            5. i15 = '1' from 1500 ns to 1600 ns
        v. Save and Simulate Behavioral Model to verify correct functionality
        * See Page 4 of this Handout for the Expected Waveform Output
    b. Synthesize with XST (look under the Process View) to verify there are no syntax errors.

Required Printouts (turned in during Demo)

Print the Grading Rubric (the last page of this hangout) and write your name and section number at the top. Then printout the four schematics listed below (make sure to add your name and section number as text to each schematic). Finally, find one of the TAs **during their Office Hours** and demo the outputs of both ModelSim simulations.

1. Schematic of 2 to 4 Decoder
2. Schematic of 4 to 16 Decoder
3. Schematic of 4 to 1 Multiplexer
4. Schematic of 16 to 1 Multiplexer

Notes

You do NOT need to checkout a Nexys2 Board for this first Computer Assignment. You are only using the software tools to build and test the designs. Future assignments will rely upon these components so make sure to keep a copy of your project's directory.

Computer Assignment #1 - Grading Rubric

Student's Name: _____ Section Number: _____

Provided printouts of the schematics:

- ☐ Schematic of 2 to 4 Decoder _____ / 4 Points
- ☐ Schematic of 4 to 16 Decoder _____ / 4 Points
- ☐ Schematic of 4 to 1 Multiplexer _____ / 3 Points
- ☐ Schematic of 16 to 1 Multiplexer _____ / 4 Points

Demo of the simulations:

- ☐ Simulation of 4 to 16 Decoder in ModelSim _____ / 5 Points
- ☐ Simulation of 16 to 1 Multiplexer in ModelSim _____ / 5 Points

Total _____ **/ 25 Points**

Expected Simulation Output

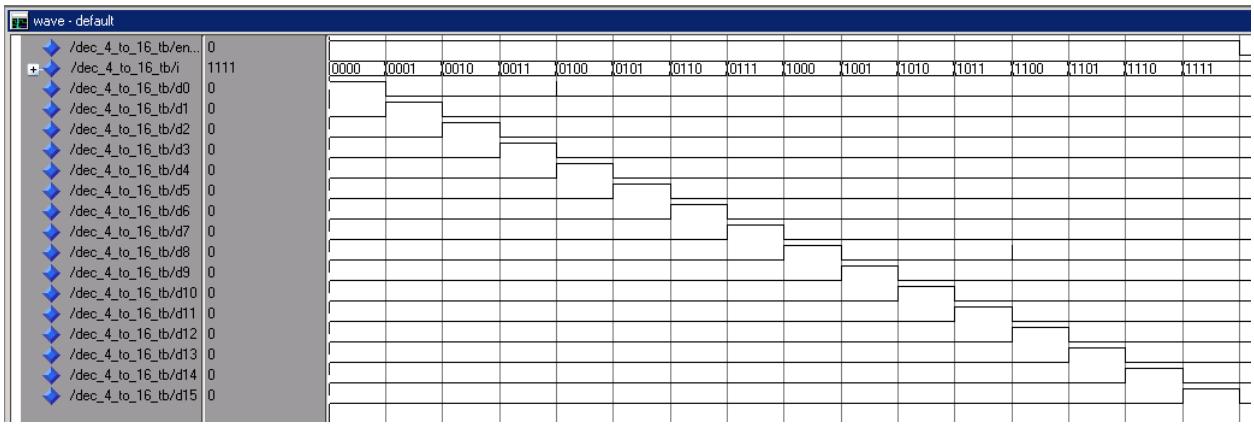

Figure 1: Expected Output from Simulation of 4 to 16 Decoder

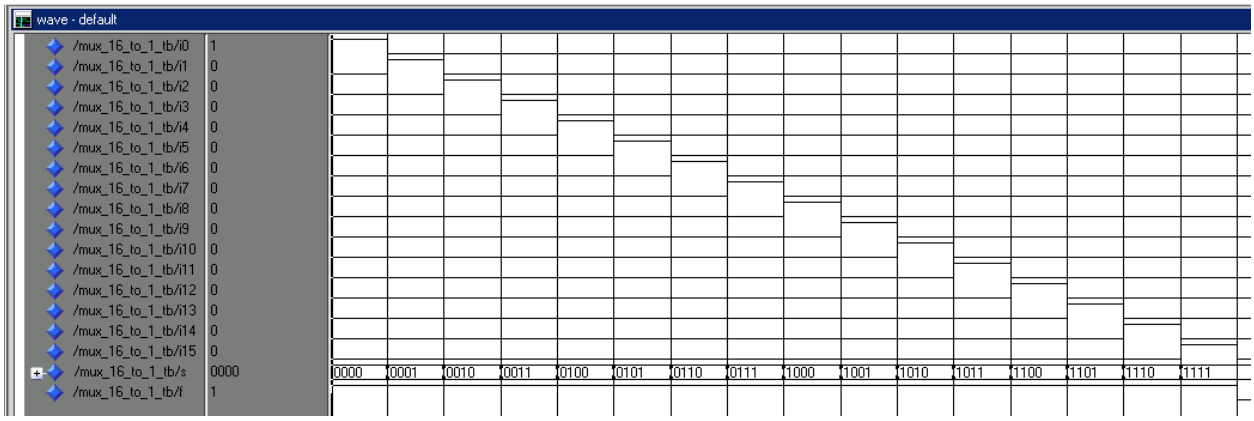

Figure 2: Expected Output from Simulation of 16 to 1 Multiplexer