Outline for 9/24/2009

Decoders - slides from pp ← Design from Gates

Muxes - slides + design from gates

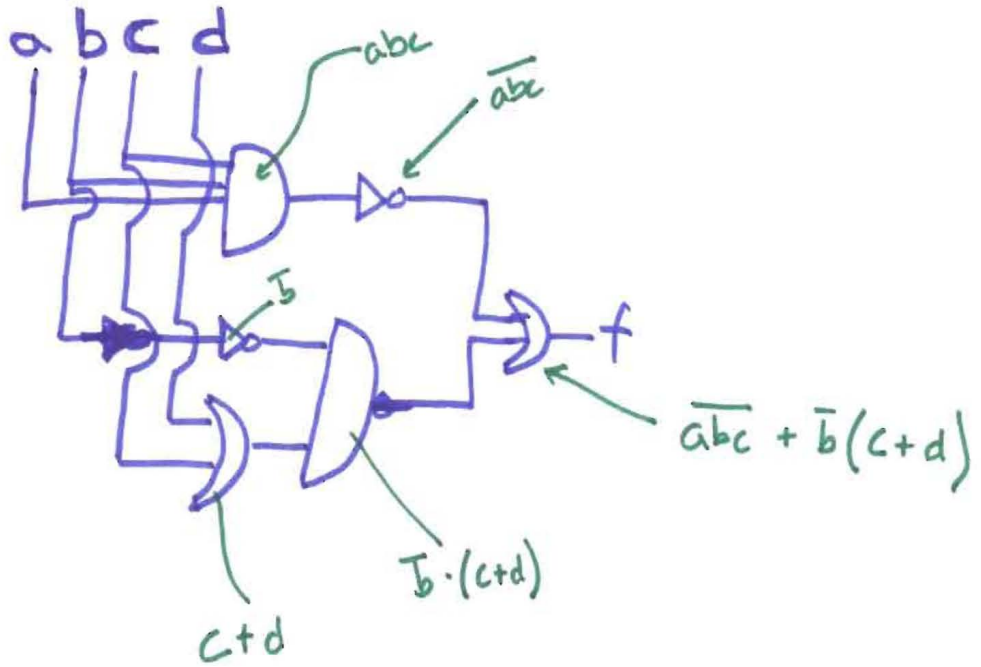
- Look into slides from both pp and supplement 2A notes

Finish ch. 2

Example of converting a circuit to using only NAND

$f = (abc)' + b'(c+d)$

original form:

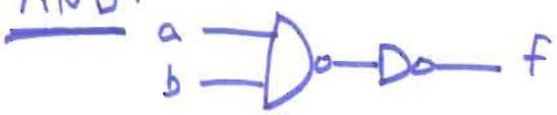


NAND Form

Not: a → $\bar{a}$

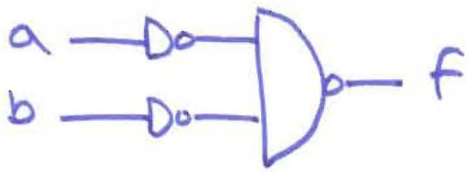
a → $\bar{a}$ 1 input NAND

AND:



2 NAND gates
1: NAND A B
2: "Not" of NAND Gate 1

OR:



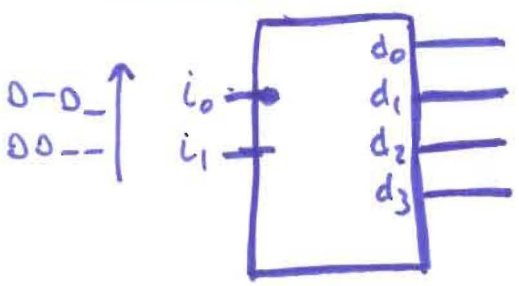
3 NAND Gates
2: a + b inputs to convert (negate)
1: NAND $\bar{a}$ $\bar{b}$ together

See truth Table

a	b	$\bar{a}$	$\bar{b}$	$\bar{a}\bar{b}$	$\overline{(\bar{a}\bar{b})} = f$	a+b
0	0	1	1	1	0	0
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	0	1	1

SAME!

Decoder



$d_0 = 1$ when $i_0 = 0$, $i_1 = 0$ else ∅

$d_1 = 1$ when $i_0 = 1$, $i_1 = 0$ else ∅

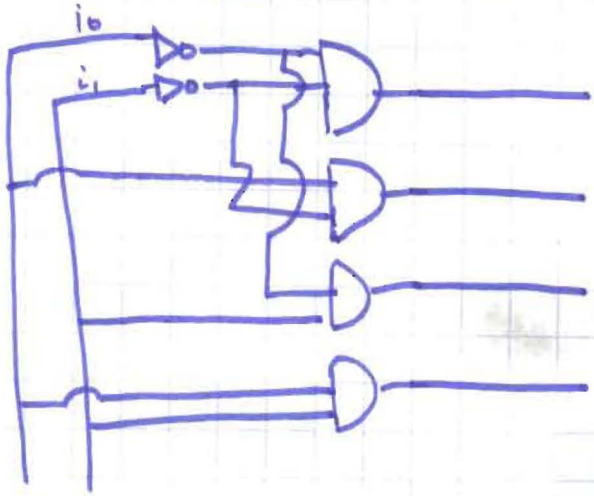
$d_2 = 1$ when $i_0 = 0$, $i_1 = 1$ else ∅

$d_3 = 1$ when $i_0 = 1$, $i_1 = 1$ else ∅

Go to Gates based on This

2^N = outputs
N = Number of inputs.

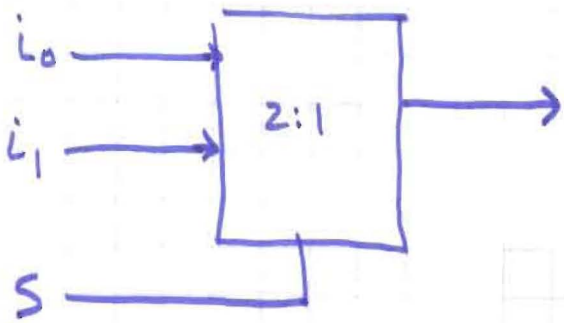
Decoder



i_0 i_1

Start with just d_0 and build around it to get d_1, d_2 and d_3

MUX: 2:1 (1-bit)



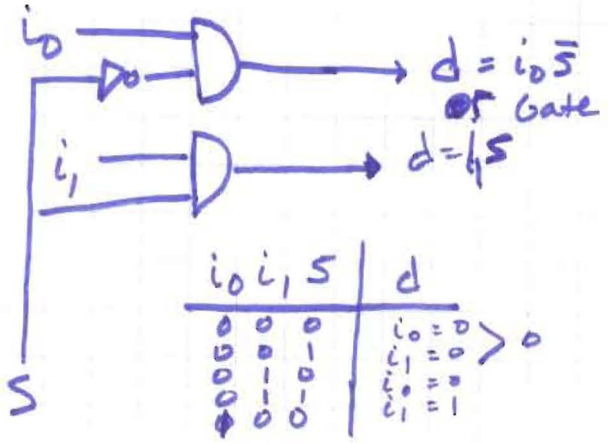
$d = i_0$ when $S = 0$
$d = i_1$ when $S = 1$

inputs compared to output Select bits

2^N = # inputs where N is # of Select bits

$2^1 = 2$

1 select bit, 2 inputs
Always 1 output



$2^2 = 4:1$ MUX

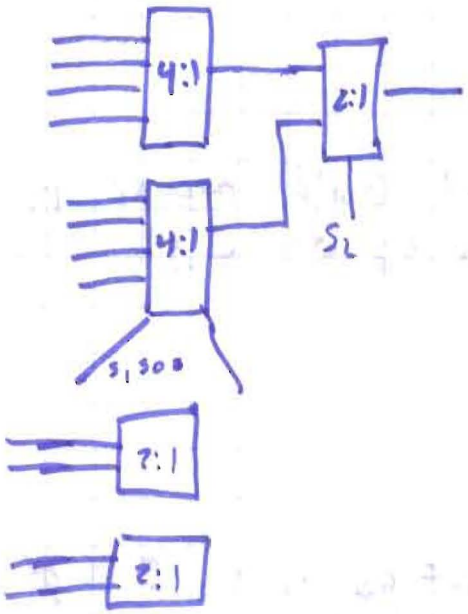
draw Truth table →

2:1 2 bit mux

4:1 1 mux

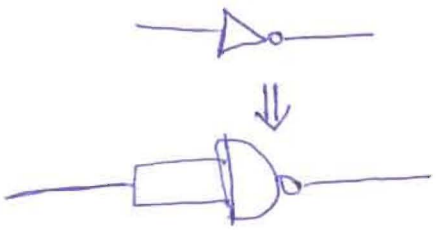
8:1 mux

made with 2:1 mux

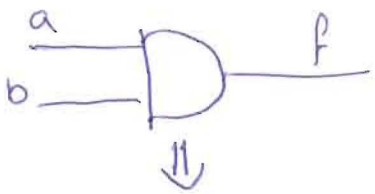


Show how to use 2:1 to build bigger muxes

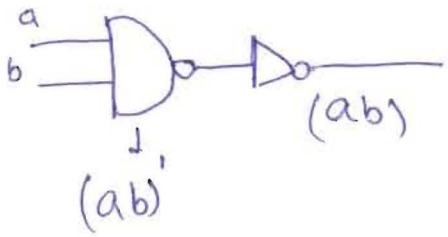
NOT Gate:



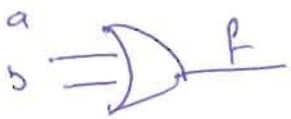
AND Gate:



~~f = a.b~~ $f = a.b$



OR gate:

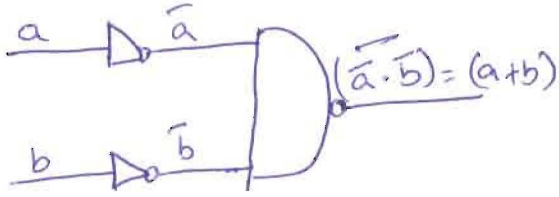


a	b	$\bar{a}$	$\bar{b}$	$\bar{a}.\bar{b}$	$\overline{(\bar{a}.\bar{b})}$
0	0	1	1	1	0
0	1	1	0	0	1
1	0	0	1	0	1
1	1	0	0	0	1

$\bar{a}\cdot\bar{b} = \overline{(a+b)}$ - I

$\overline{ab} = \bar{a}+\bar{b}$ - II

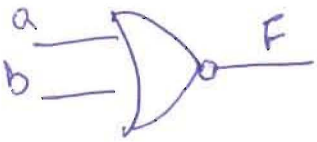
$\Rightarrow$



Consider I:

$\overline{(\bar{a}\cdot\bar{b})} = \overline{(\bar{a}+b)} = \underline{a+b}$.

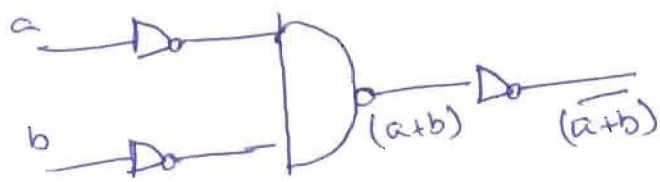
NOR Gate:



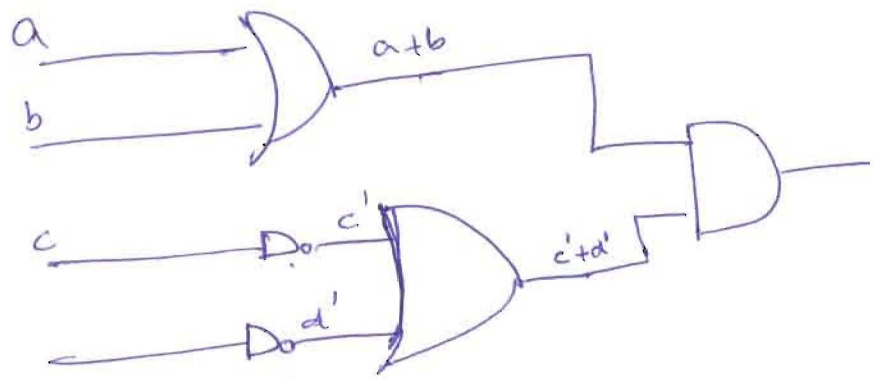
NAND

a	b	$\bar{a}$	$\bar{b}$	$\overline{(\bar{a}\cdot\bar{b})}$	$\overline{\overline{(\bar{a}\cdot\bar{b})}}$
0	0	1	1	0	1
0	1	1	0	1	0
1	0	0	1	1	0
1	1	0	0	1	0

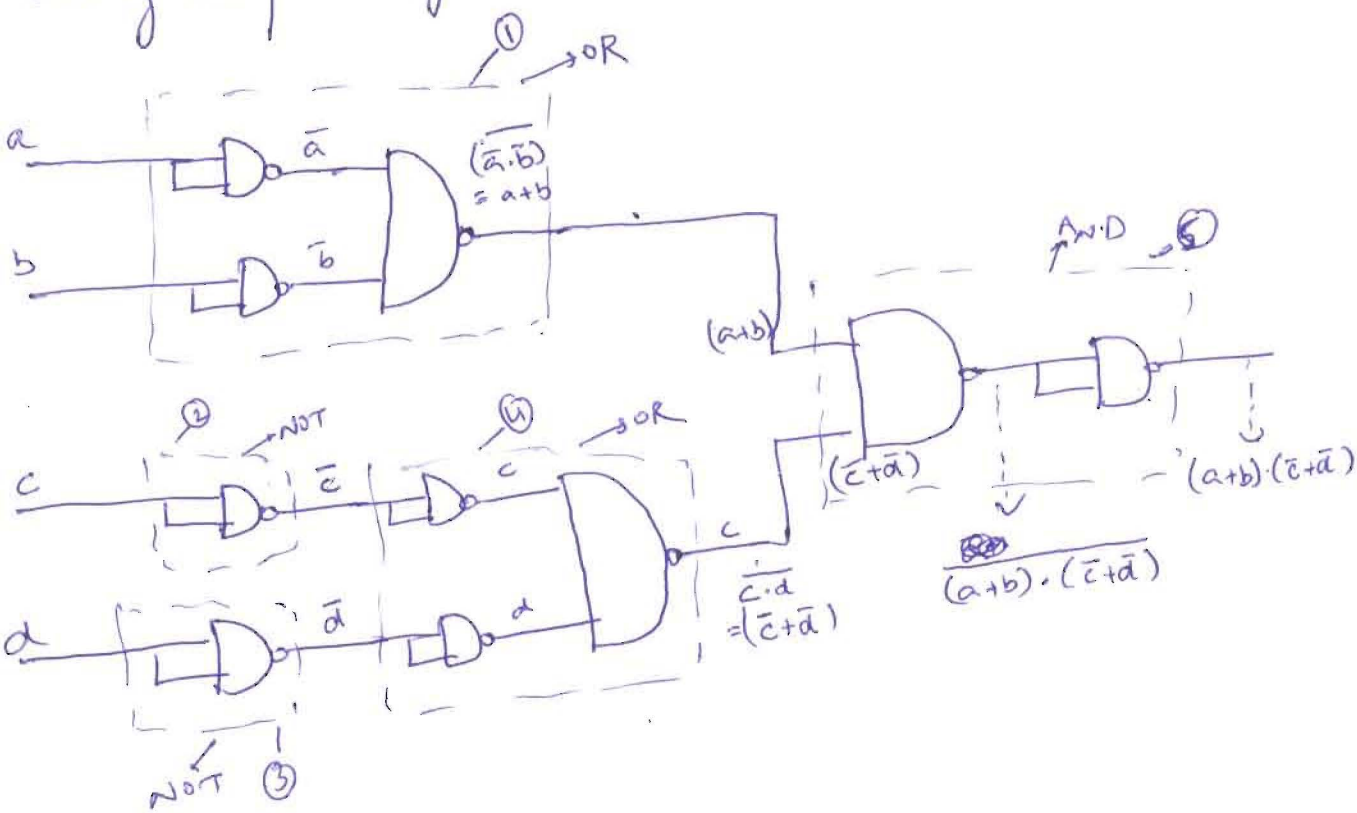
$\overline{\overline{(\bar{a}\cdot\bar{b})}} = \bar{a}\cdot\bar{b} = \overline{(a+b)}$ – for equation II

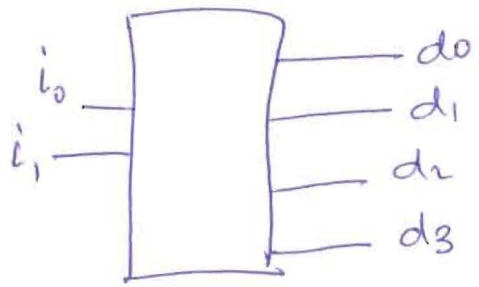


$(a+b)\cdot(c'+d')$



Using only NAND gates:

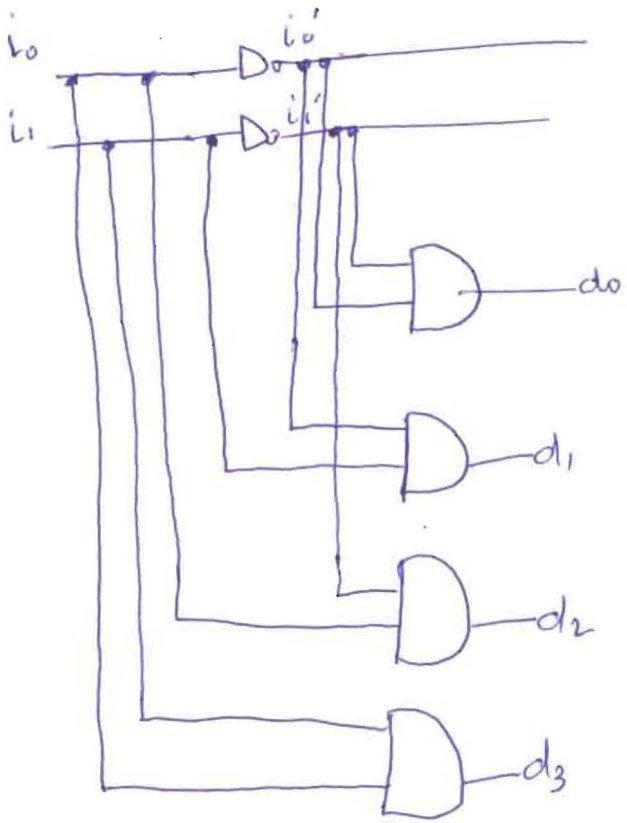




i_0	i_1	output selected
0	0	d_0
0	1	d_1
1	0	d_2
1	1	d_3

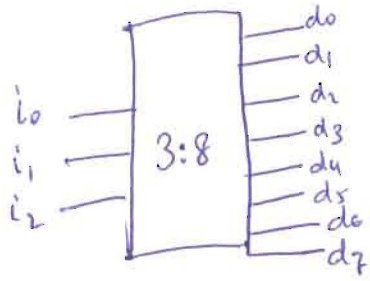
i_0	i_1	output
0	0	d_0
0	1	d_1
1	0	d_2
1	1	d_3

$$d_0 = \overline{i_0} \cdot \overline{i_1}$$
$$d_1 = \overline{i_0} \cdot i_1$$
$$d_2 = i_0 \cdot \overline{i_1}$$
$$d_3 = i_0 \cdot i_1$$



3:8 decoder

$2^3 = 8$



i_0	i_1	i_2	output selected
0	0	0	d_0
0	0	1	d_1
0	1	0	d_2
0	1	1	d_3
1	0	0	d_4
1	0	1	d_5
1	1	0	d_6
1	1	1	d_7

$$d_0 = \overline{i_0} \cdot \overline{i_1} \cdot \overline{i_2}$$

$$d_1 = \overline{i_0} \cdot \overline{i_1} \cdot i_2$$

$$d_2 = \overline{i_0} \cdot i_1 \cdot \overline{i_2}$$

$$d_3 = \overline{i_0} \cdot i_1 \cdot i_2$$

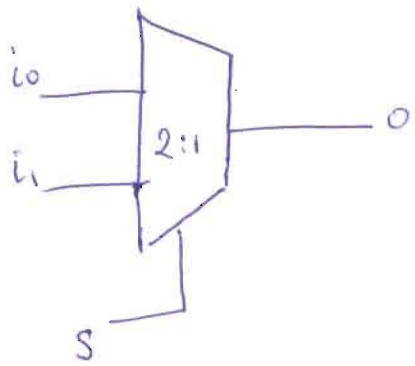
$$d_4 = i_0 \cdot \overline{i_1} \cdot \overline{i_2}$$

$$d_5 = i_0 \cdot \overline{i_1} \cdot i_2$$

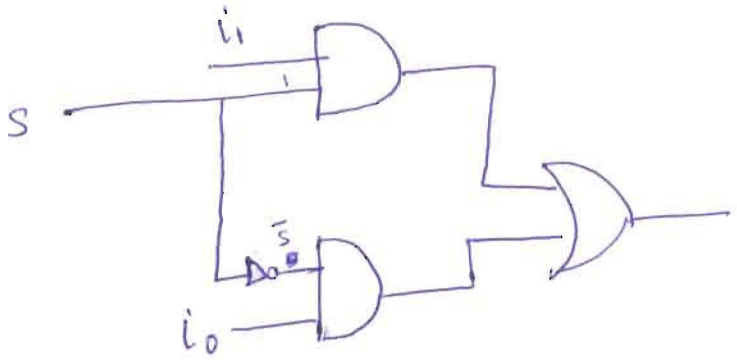
$$d_6 = i_0 i_1 \cdot \overline{i_2}$$

$$d_7 = i_0 \cdot i_1 \cdot i_2$$

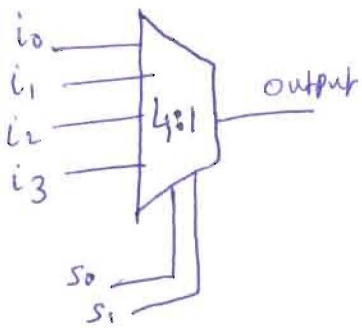
2:1 MULTIPLEXER:

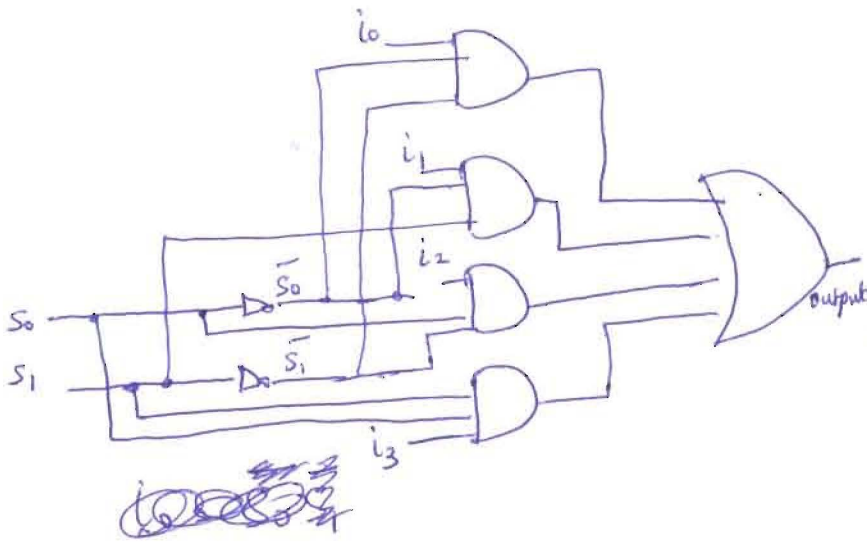


S	output (O)
0	i_0
1	i_1



4:1 MUX:





S_0	S_1	output
0	0	i_0
0	1	i_1
1	0	i_2
1	1	i_3

output = $\bar{S_0}\bar{S_1} \cdot i_0 + \bar{S_0} S_1 \cdot i_1 + S_0 \bar{S_1} \cdot i_2 + S_0 S_1 \cdot i_3$