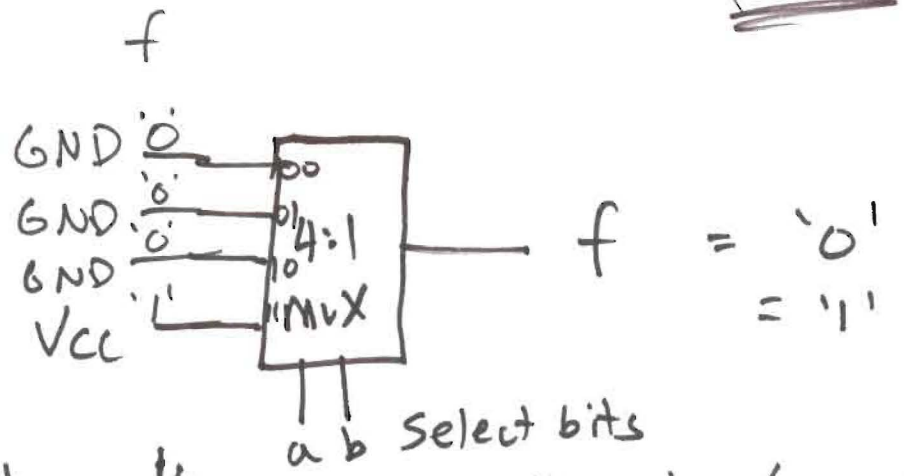
10/06/2009 Outline

- Exam #1 - 9 - 10:15 AM Oct 9th Woodward 125
- No class on oct 12/13 - Fall Break
- Hw 6 due 10/15/2009
- Grades

- Mux to build "function lookup"
- De mux
- Hardware Description Languages
  - VHDL
  - Verilog
  - SystemC

A	B	f
0	0	0
0	1	0
1	0	0
1	1	1

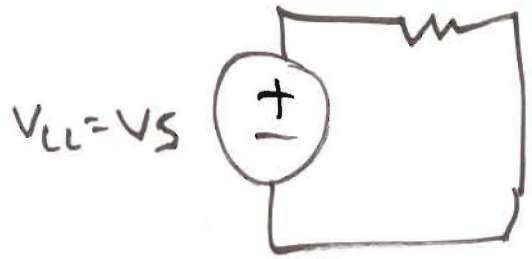
$f = AB$ (AND)



GND = '0'

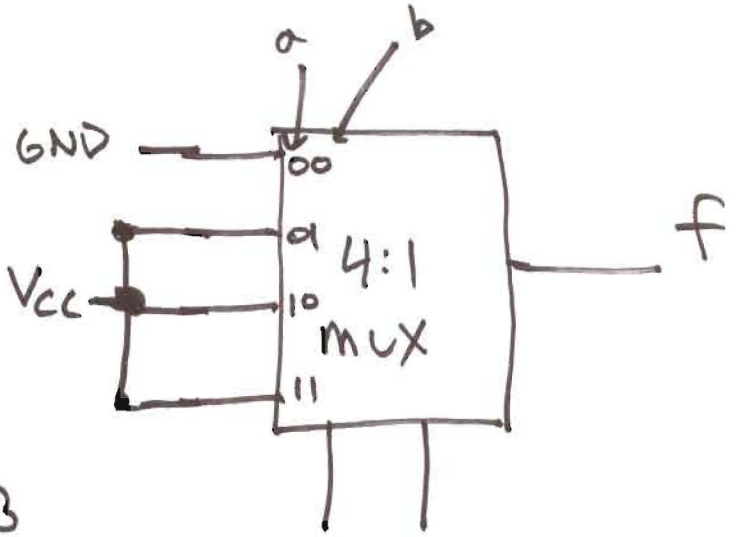
Vcc = '1'

4 input / 1 output MUX



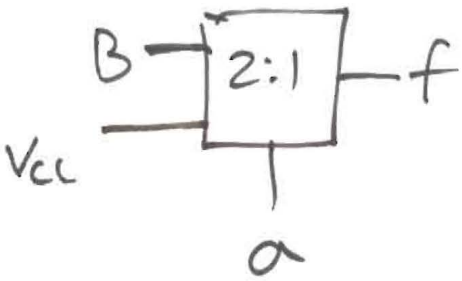
Lookup Table

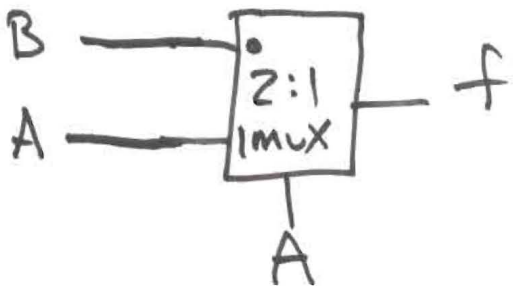
A	B	f
0	0	0
0	1	1
1	0	1 X
1	1	1



$f = \bar{A}B + A\bar{B} + AB$

Inverters





2 inputs

$\log_2(2) = 1$ select bit

A=0

f=B

A=1

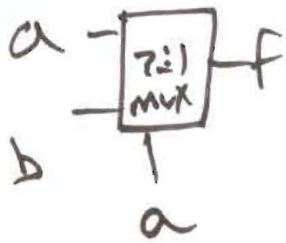
f=1 (A)

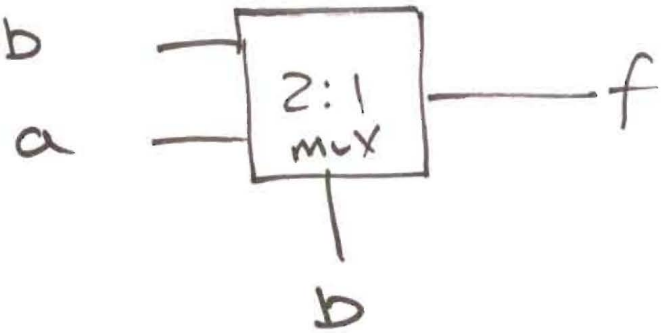
16:1 mux

$\log_2(16) = 4$

$2^4 = 16$

A [illegible] Gate from a 2:1 MUX

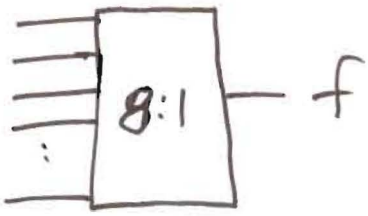




a	b	f
0	0	0
0	1	0
1	0	0
1	1	1

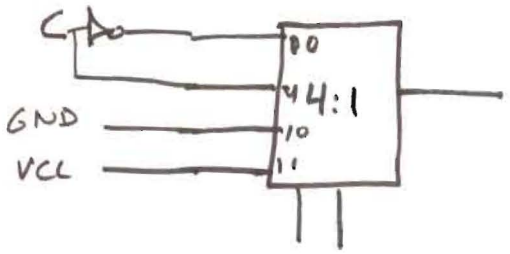
A	B	C	f
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

could do it this way...

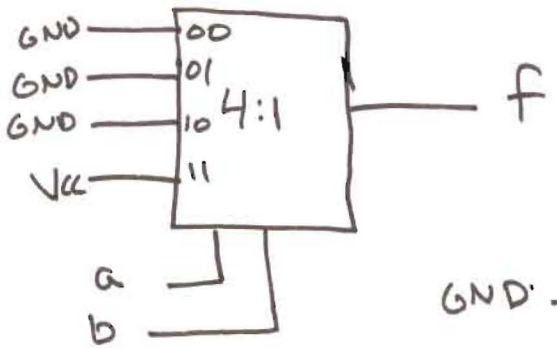


more compact

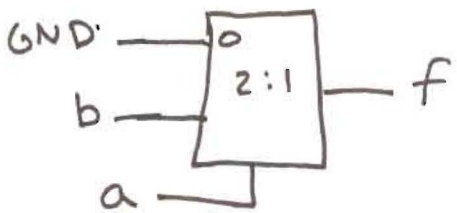
(b)



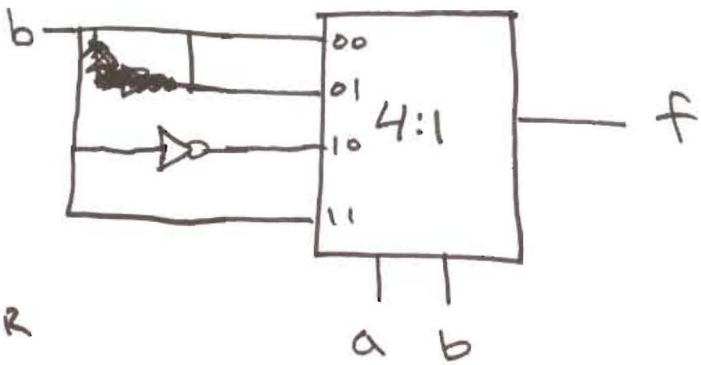
A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

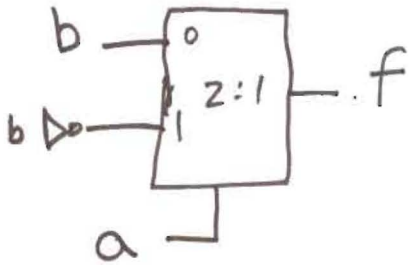


GND = '0'
Vcc = '1'
"Common Collector Voltage"



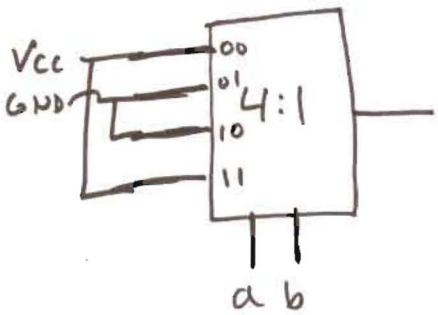
A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

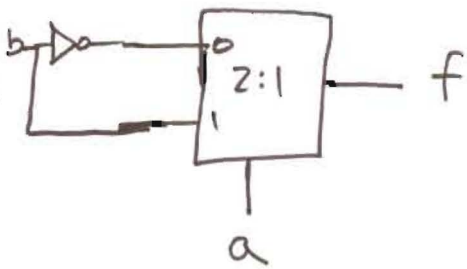


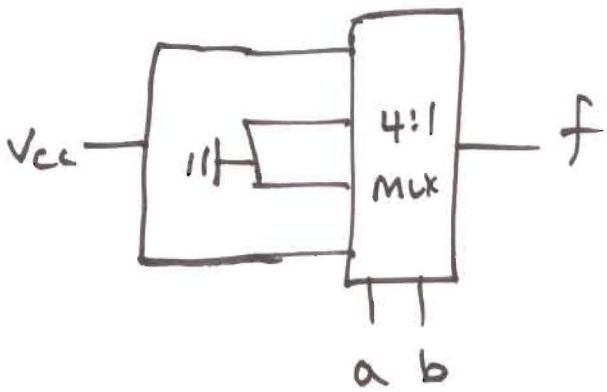


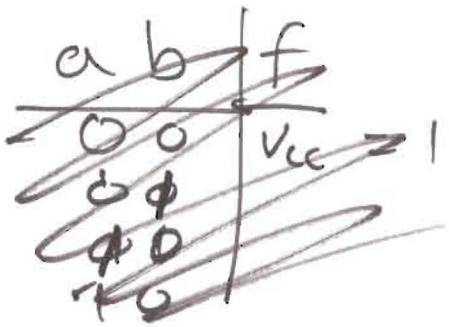
XNOR

A	B	f
0	0	1
0	1	0
1	0	0
1	1	1









a	b	f
0	0	Vcc = 1
0	1	0
1	0	0
1	1	1

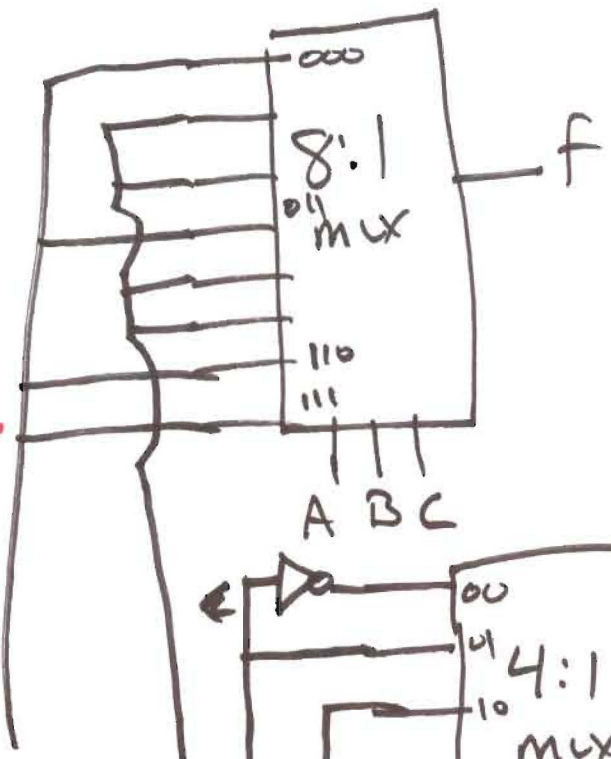
XNOR ?

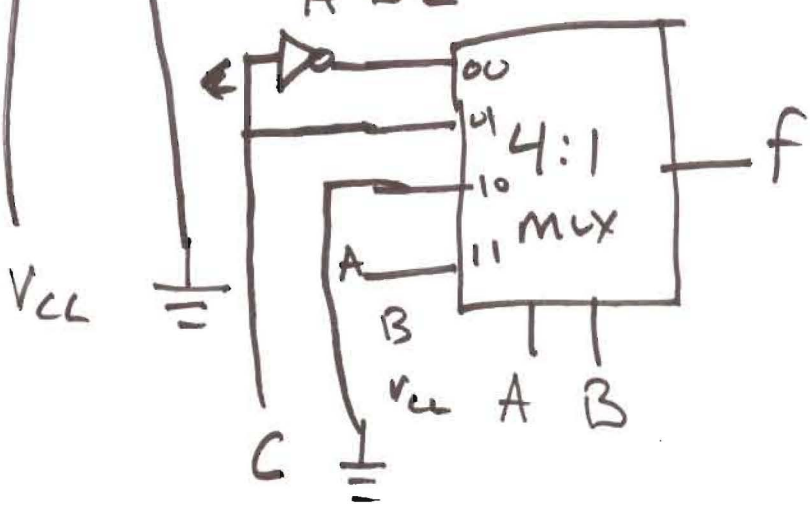
0	0	1
0	1	0
1	0	0
1	1	1

XOR

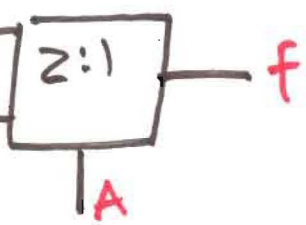
0
1
1
0

A	B	C	f
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

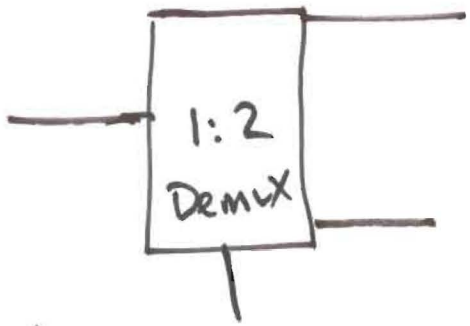




AND A XNOR C
OR
NOT B



Demux



1 input

2 outputs

1 select

1:4