Outline for 10/8/2009

- Exam on Friday!
- HW 6 due 10/15/2009
- 10/16/09 Recitation to be at 8 AM
  for Computer Assignment Tutortial
- Ch. 9 VHDL + Verilog Slides

<u>VHDL</u>

```
Entity Inv is
  Port ( X; in std-logic
         F : out std-logic
       );
end entity inv;
```

<u>Verilog</u>

```
module inv (X, F);
   input X;
   output F;
end modlle
```

Process

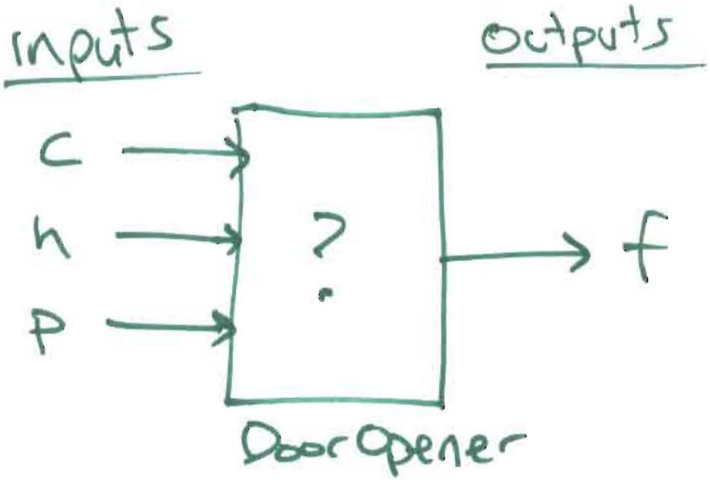
Always Block

Post Notes & check

//

/*

*/



comment

VHDL

```
entity DoorOpener is
port (  c : in  std_logic;   --(bit)
        h : in  std_logic;   -- '0'
        p : in  std_logic;   -- '1'
        f : out std_logic
);
```

$$f(x, y, z) = x + y \cdot z$$

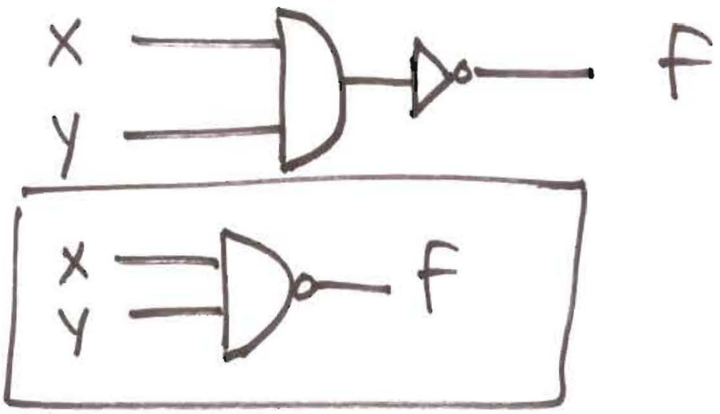
no comma

NAND

"Not" AND

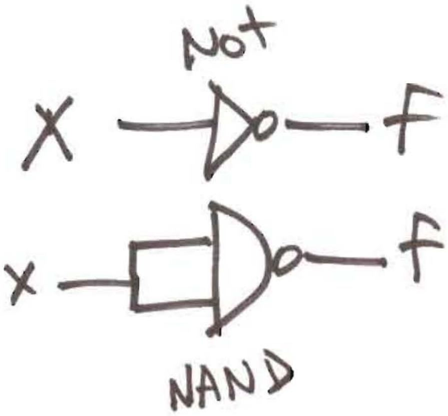
X	Y	X NAND Y	
0	0	1	Not 0
0	1	1	
1	0	1	
1	1	0	Not 1

X	Not
0	1
1	0

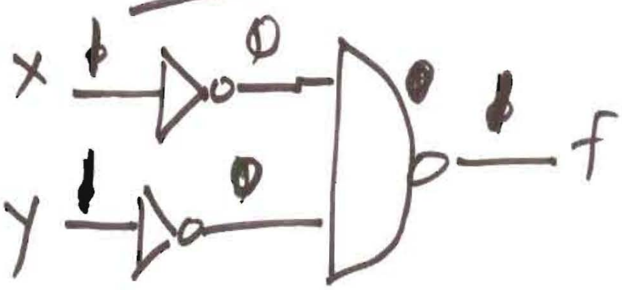


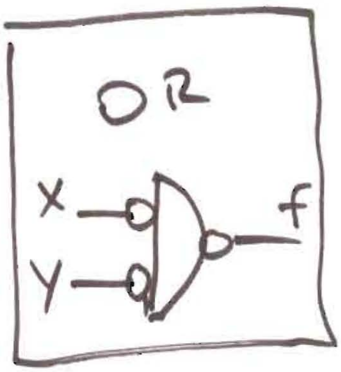
f

X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1



OR





NOR Not OR

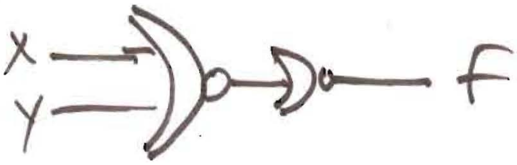
X	Y	OR	NOR	AND
0	0	0	1	0
0	1	1	0	0
1	0	1	0	0
1	1	1	0	1

OR NOR

NOR to Create a Not Gate

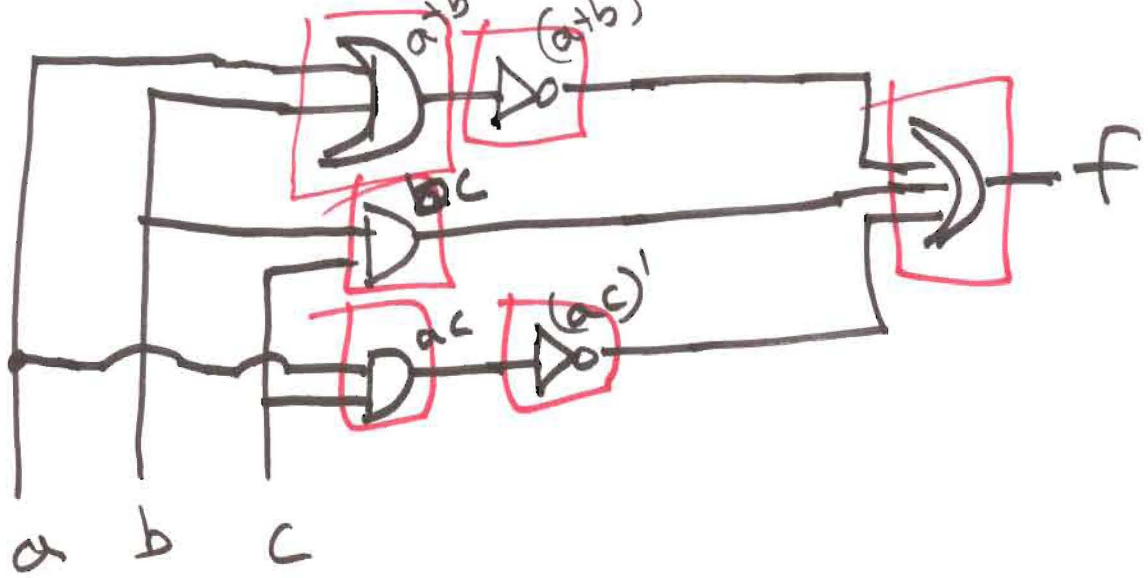
AND

OR

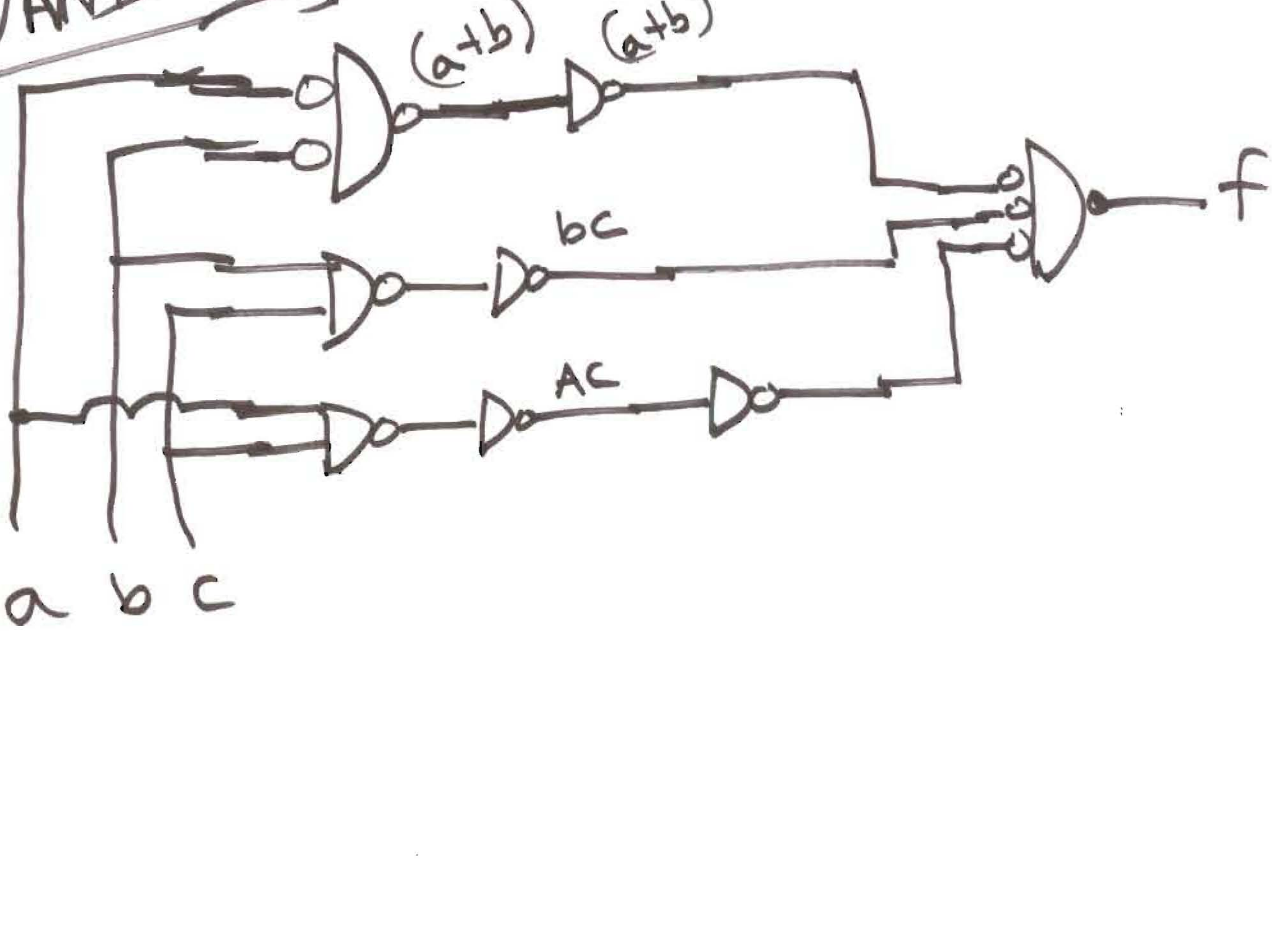


$$f(a,b,c) = (a+b)' + bc + (ac)'$$

~~NAND~~



NAND only



$a'b' + bc + a' + c'$

$a'(b' + 1) + bc + c'$

$a' + \underline{bc + c'}$

$a' + (c' + b) * (c' + c)$

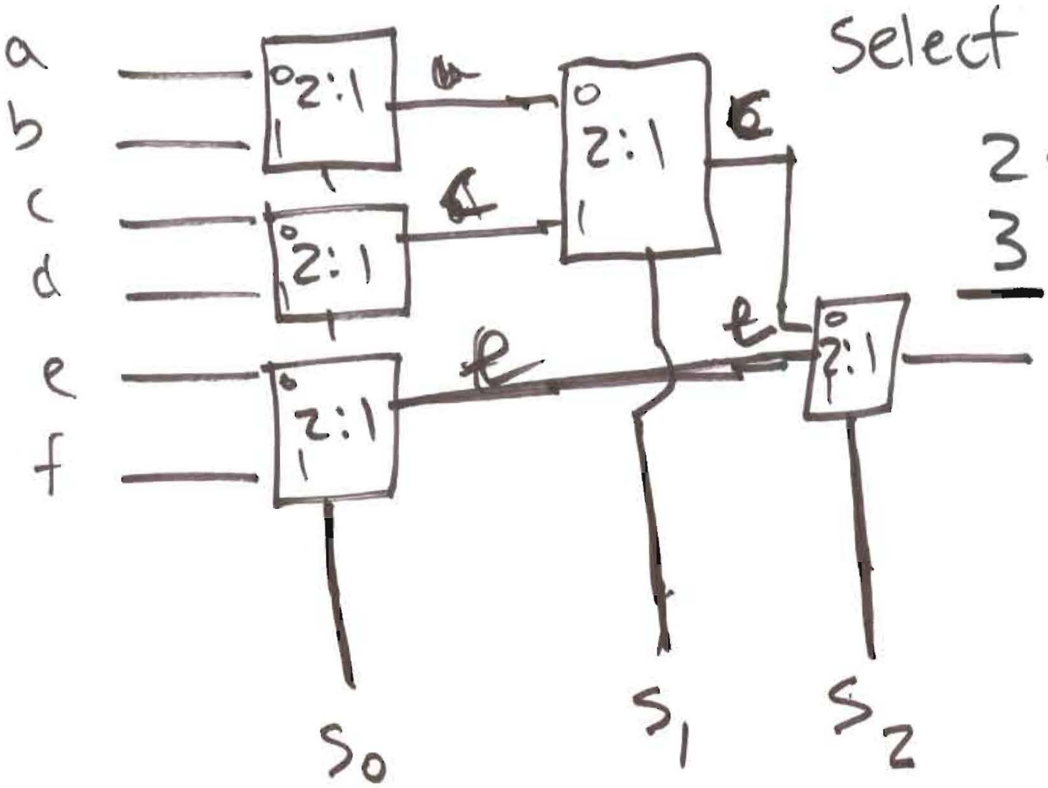
$a' + c' + b \quad$ 1 comp, 1d

$\boxed{a' + c' + b}$

2 - Not

1 - OR

6:1 mux   2:1 mux



Select Lines

2 - 4 inputs
3 - 8 inputs

f = f

s_0	s_1	s_2
1	0	1
0	1	$\cancel{0}$

000
$s_2 s_1 s_0$
101 —
110 —
111 —

0 - 5 : a - f
6 + 7 : (?)

0
7E   7
0111 1110   8
x00 7E
FFFE

0x16
16   F   E

0xFE   1111   1110   0b1011
1011

16_{16} 16_{10}