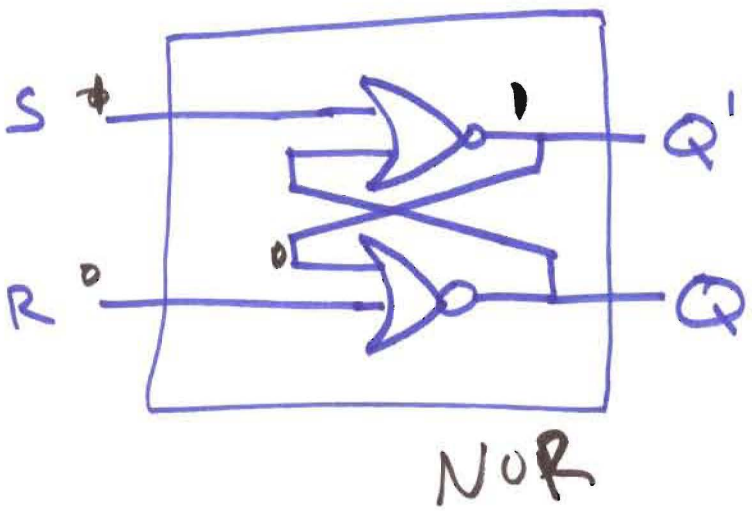
11/12/09 outline

1) HW 10 due ~~11/17 - Tuesday~~ 11/18 - Wednesday - Conrad
   11/19 - Thursday - Schmidt
2) Exam 2 - 9 AM 11/20
3) Recitation - 8 AM Review
4) Draw
   - SR Latch
   - Level Sensitive SR Latch
   - Level Sensitive D Latch
   - D Flip Flop
5) Timing Examples

1) Draw The SR LATCH

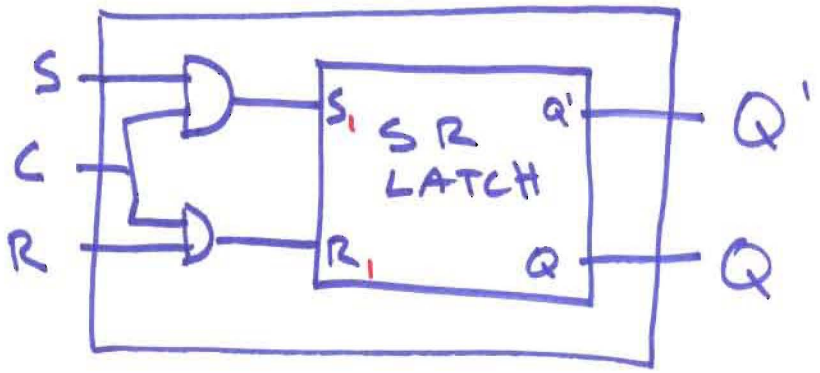


NOR

S	R	Q	Q'
0	0	0	1
0	1	0	1
1	0	1	0
★ 1	1	X	X

Signals: set - S
Reset - R
Q - output
Q' - inverse Q

2) Draw The "Level" Sensitive SR LATCH

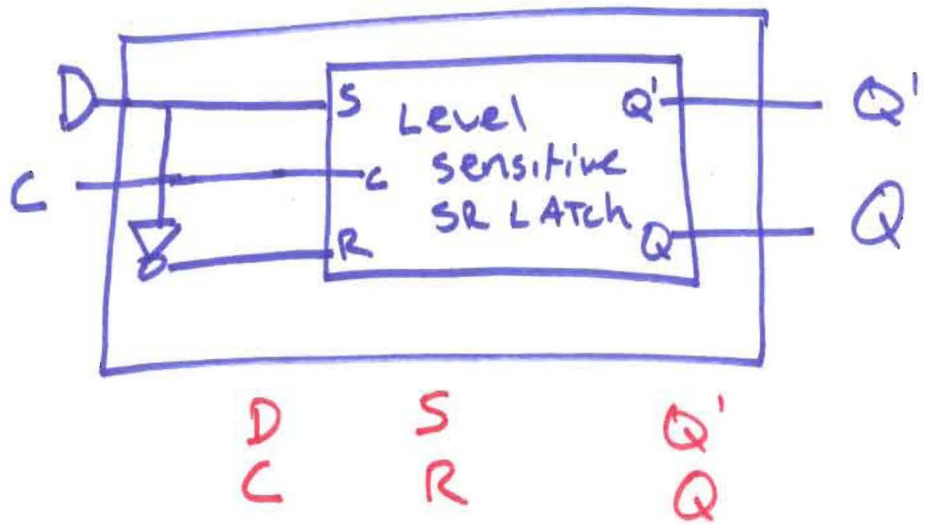


S
C
R

internal S_1
R_1

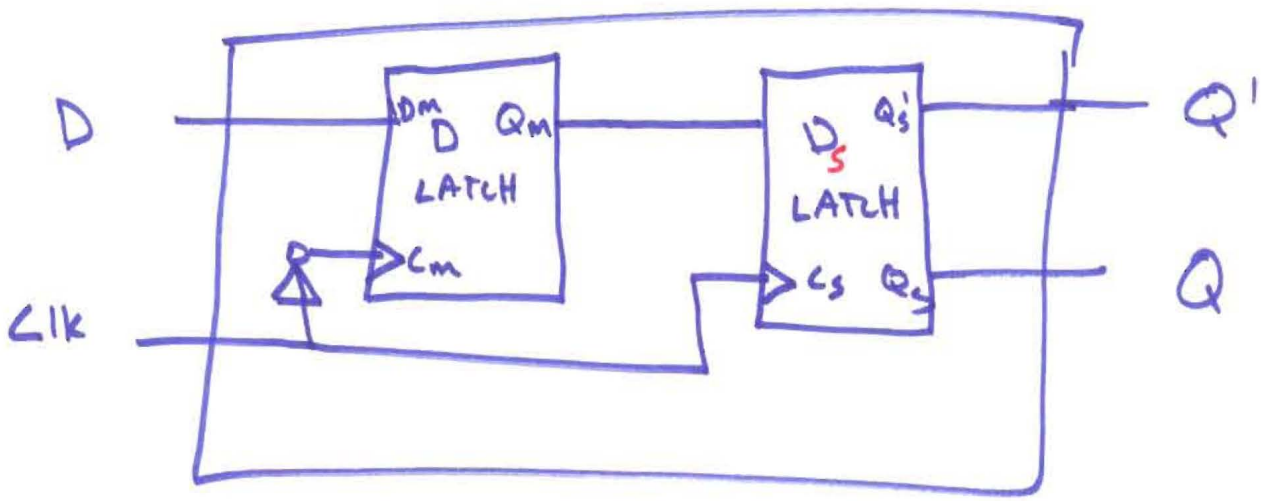
output Q'
Q

3) Level Sensitive D-Latch



D S Q'
C R Q

4) D Flip Flop



D/Dm

Clk/Cs

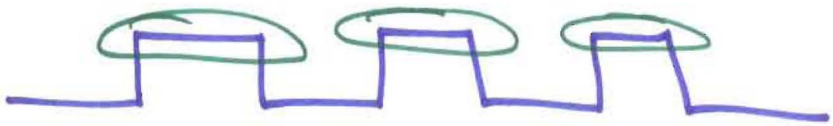
Cm = not(clk)

Qm/Ds

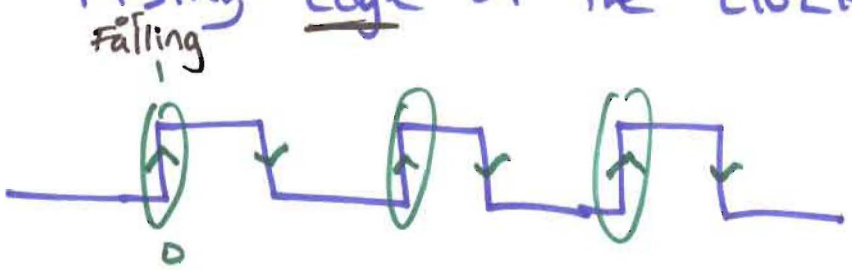
Q/Qs

Q'/Qs'

Latch: Stores the bit value on the level of the clk



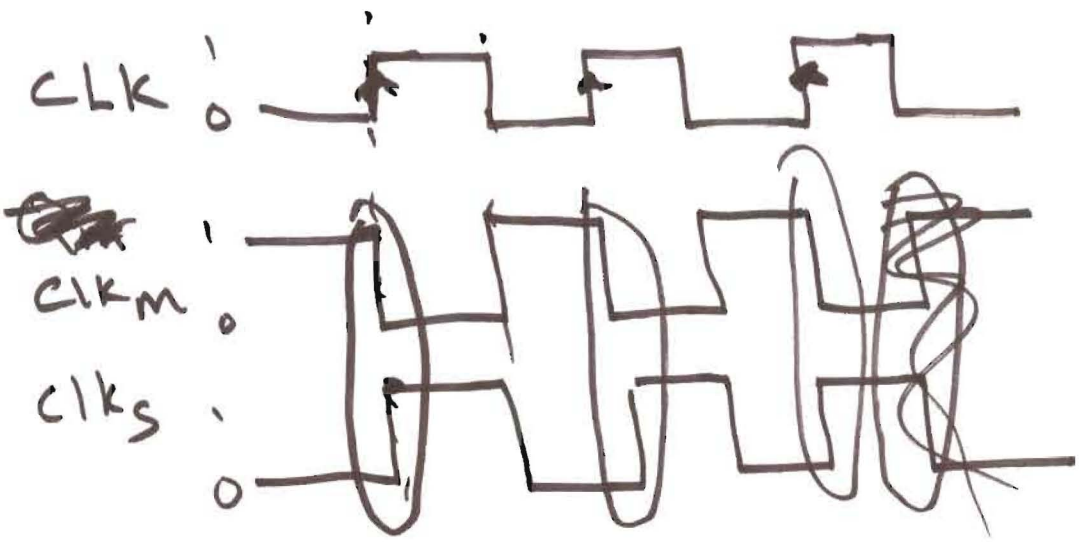
Flip-Flop: Store the bit value on the rising edge of the clock



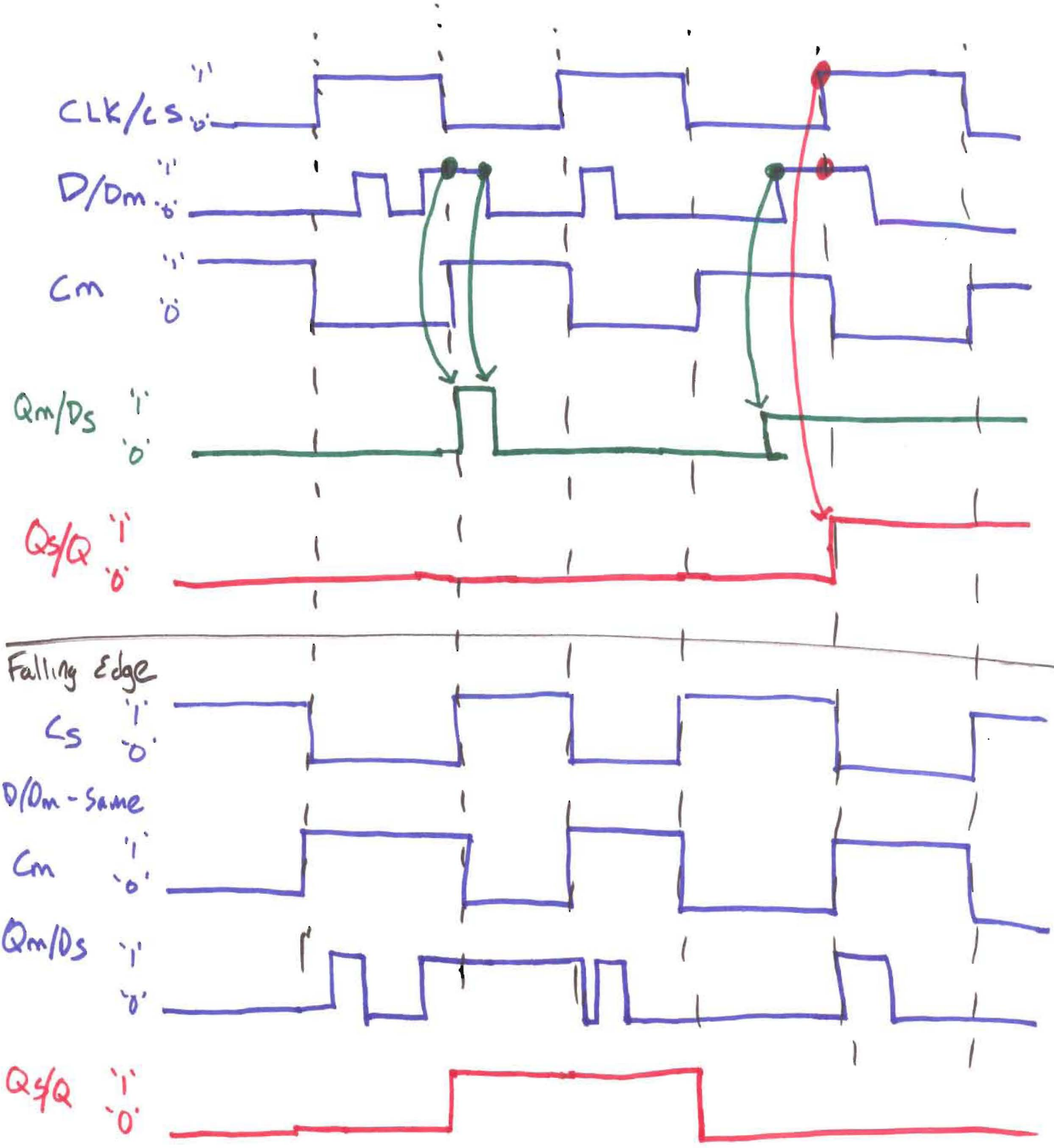
Latch

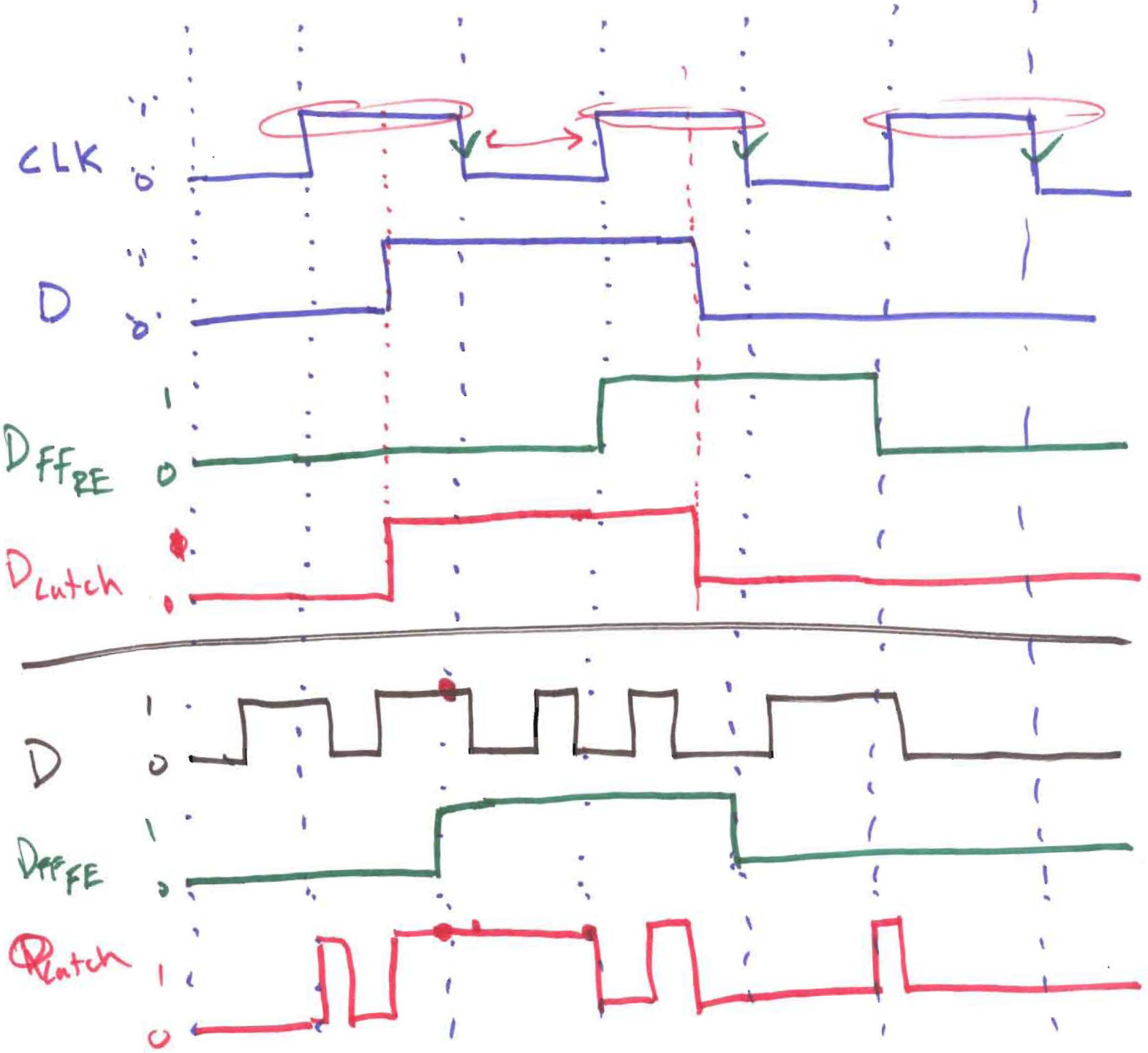
Input is neg

Input is positive



D Flip Flop @ Rising Edge Clk




CLK
D
$D_{FF_{RE}}$
D_{Latch}
D
$D_{FF_{FE}}$
D_{Latch}