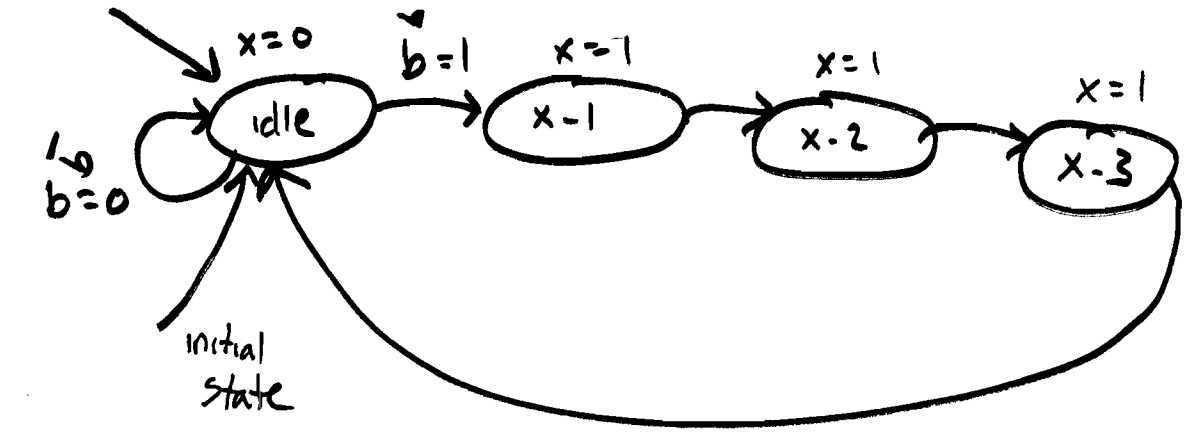
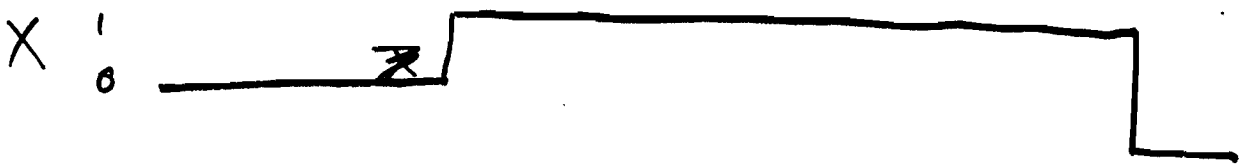
Finite State Machine

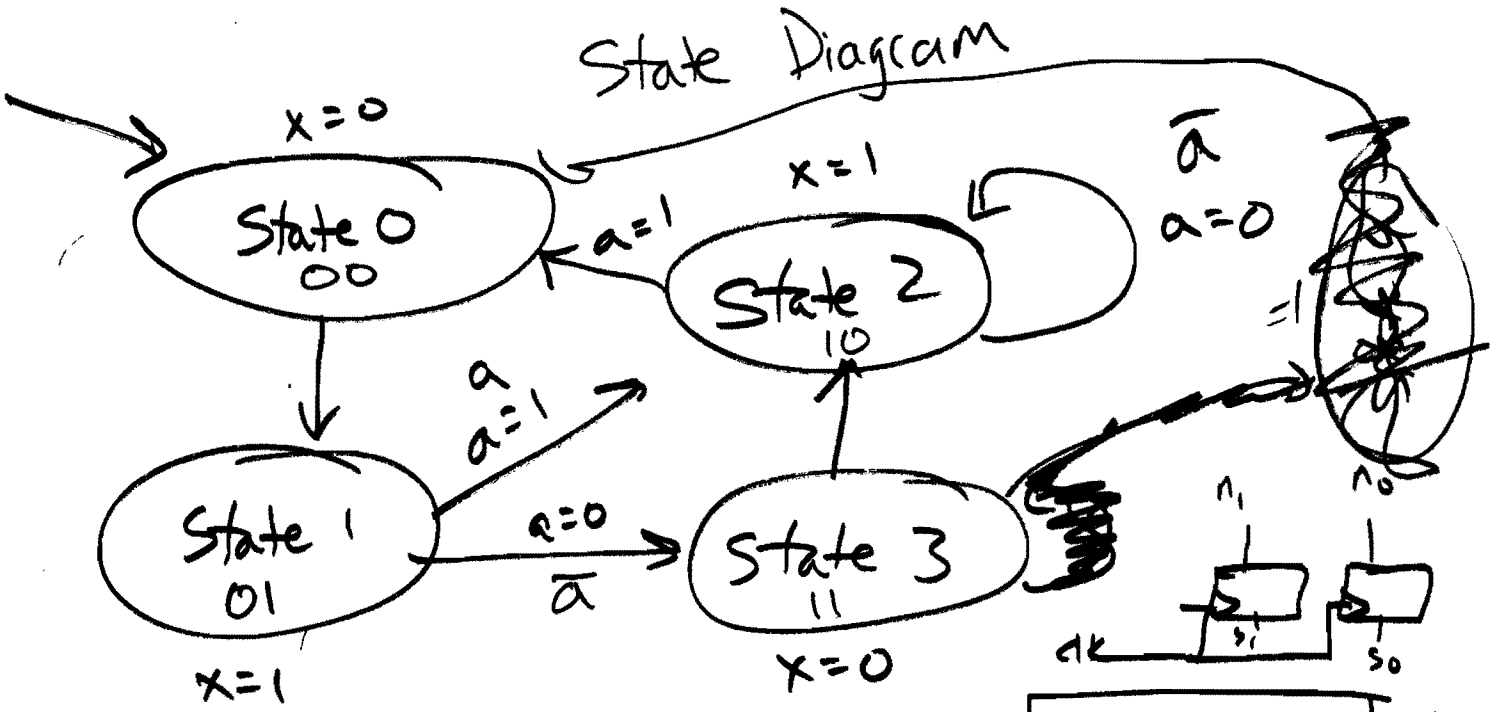
x=0
wait for b = 1
then
x=1 for 3 clock cycles

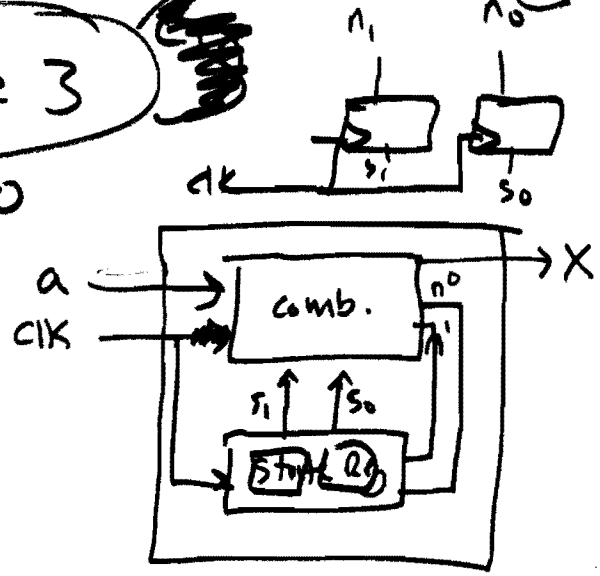
x - output
b - input
clk





State Diagram





initial state – State ∅

output – X

input – a

States: State ∅ (00), State 1 (01), State 2 (10), State 3 (11)

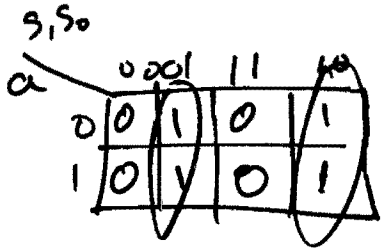
4-States

2-bits $S_1\ S_0$ - current state

$n_1\ n_0$ - next state

State Table

	inputs			outputs		
	a	S_1	S_0	a	X	n_1	n_0
State ∅	0	0	0	0	0	0	1
	1	0	0	1	0	0	1
State 1	0	0	1	0	1	1	1
	1	0	1	1	1	1	0
2	0	1	0	0	1	1	0
	1	1	0	1	0	0	1
3	0	1	1	0	1	1	0
	1	1	1	1	0	1	0



$X = \bar{S}_1 S_0 + S_1 \bar{S}_0$

FSM

a=1

1001

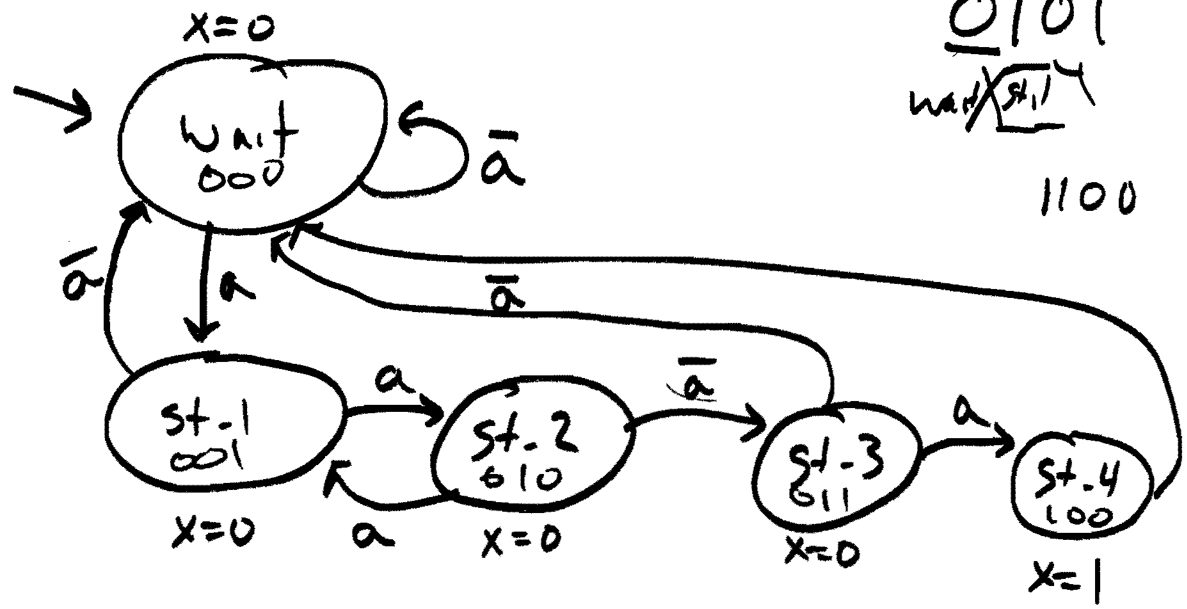
A - input

X = 1 when we detect the sequence

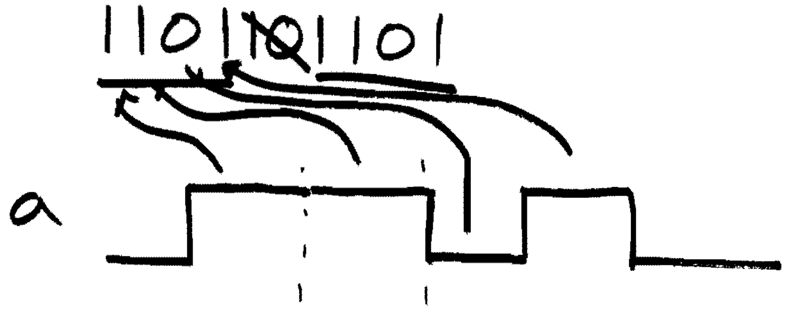
A → 1101 match

111101

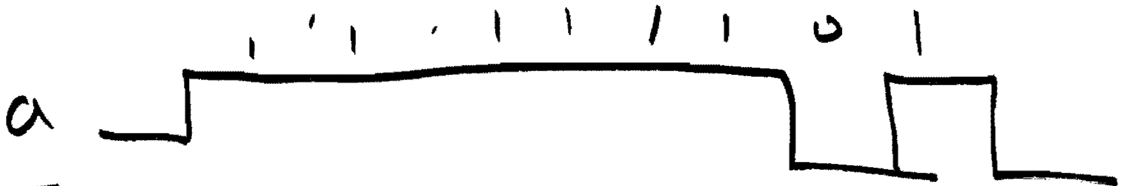
0101



1100



10001



1 0 0 0 | 1 00

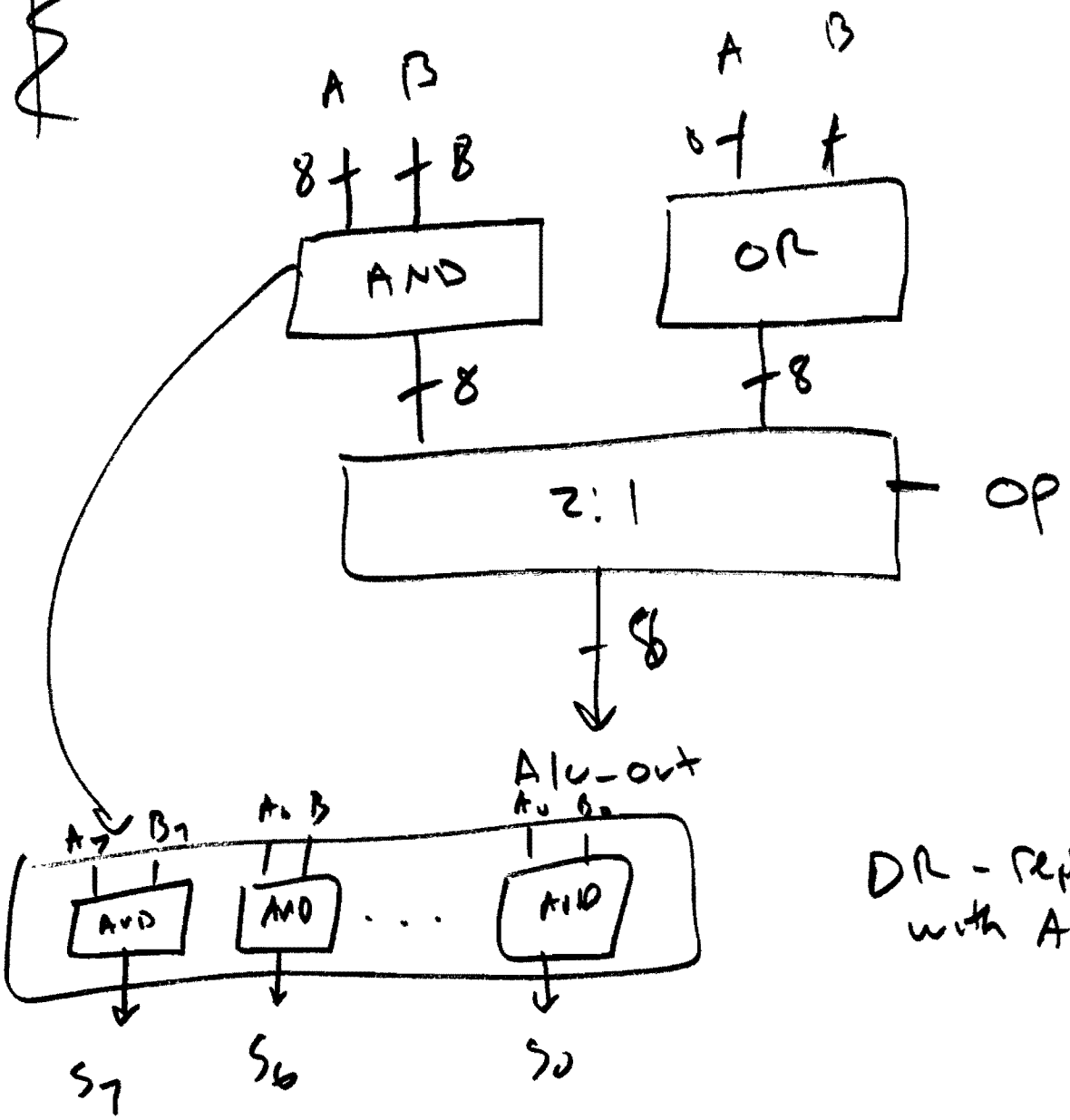
1 1 0 0 1 | 1 00

X X X X X Y

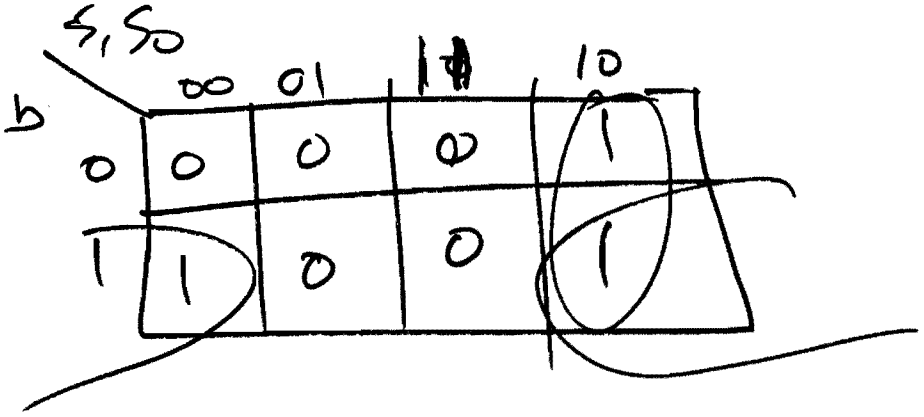
OP	
0	A AND B
1	A OR B

2 - operations
1 - OP bit

ALU



OR - replace with AND



$$n_0 = S_1\overline{S_0} + \overline{S_0}b$$

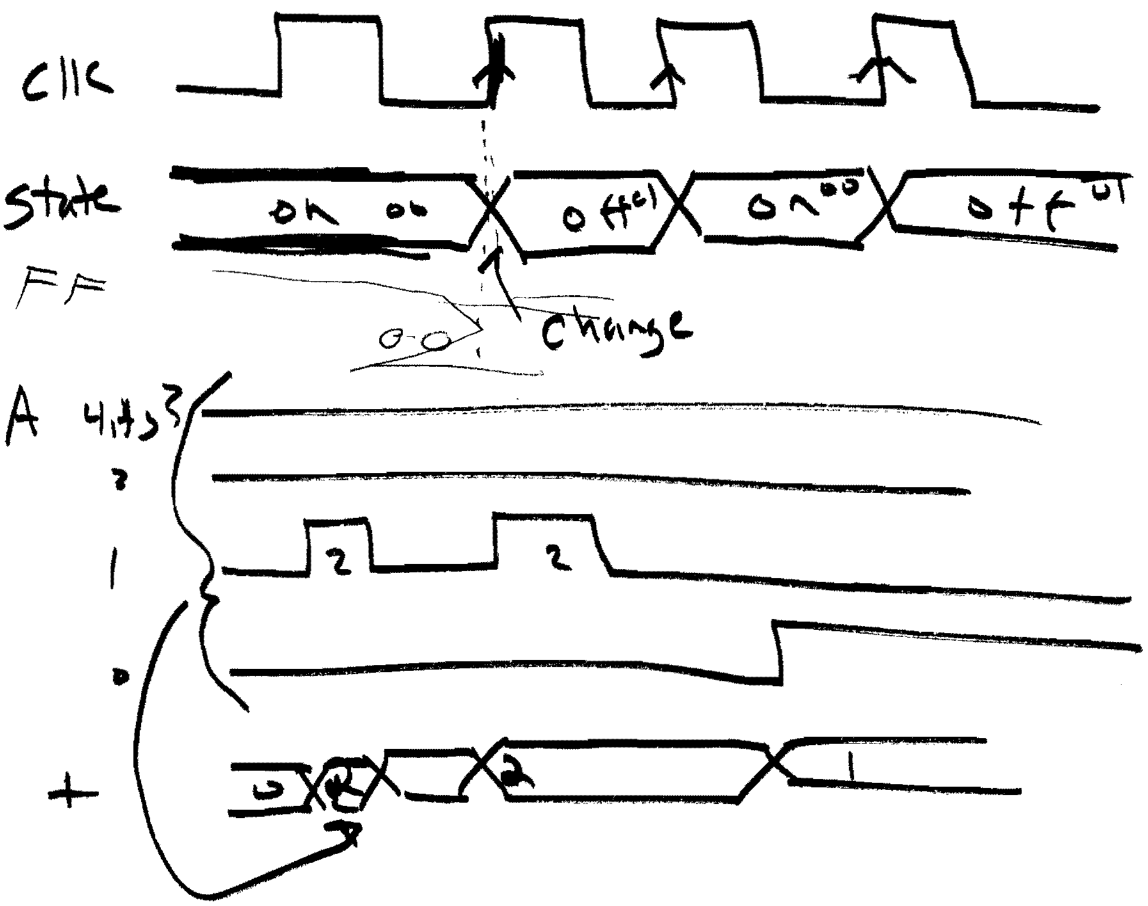
Bitwise

A = 1 0 0 1

B = 0 0 1 1

BW. AND: 0 0 0 1

OR: 1 0 1 1



bus -
multiple bit
signal