Computer Assignment 1

ECGR 2181 - Fall 2015 – Version 1.1

Assignment Overview

In this assignment you will use Vivado 15.2 Webpack to write and simulate some simple VHDL files. There are two main tasks in this assignment. The first being a simple AND gate and the simple being a slightly more complete circuit. Using the techniques learned in class and from the tutorial, complete both tasks. You'll also need to turn in a single PDF to Moodle (instructions below).

Getting started

1. Create a directory to store all of the assignment's files.
2. Open Vivado 2015.2 and create a new project called **computer_assignment_1**.
3. It will be an RTL project
4. No sources to input. Although if the target and simulation languages aren't set to vhdl, change them to vhdl.
5. No existing IP.
6. No constraints file.
7. The Basis3 uses an **XC7A35T-1CPG236C** FPGA
    - Artix 35T
    - Speed grade 1
    - CPG236 packaging
    - C temp grade

Task 1

This task is to implement the function ***Y = A and B*** in task1.vhd. It may seem trivial but it's a good starting point. Make sure to read the instructions before starting.

1. Add the task1.vhd file:
    a. Under "Flow Navigator" click "Add sources."
    b. Select "Create or add design sources."
    c. Add task1.vhd and then click "Finish."
2. Once you have your vhdl source file, edit it to implement the function.
3. Make sure it's syntax error free and can be synthesized.
4. Add the task1_tb.vhd file:
    a. Under "Flow Navigator" click "Add sources."
    b. Select "Create or add simulation sources."
    c. Add task1_tb.vhd.
    d. Make sure simulation set is "sim_1."
    e. Click "Finish.
5. Select the right simulation set:
    a. Under "Flow Navigator" click "Simulation Settings."
    b. Under "Simulation set" input "sim_1."
    c. Under "Simulation top module name" input "task1_tb."

    d. Click “Ok.”
6. Run the simulation by and check your results. The expected output is on the last page of the assignment.
7. Vivado doesn’t include a way to print test bench results so you will have to take a screenshot.

Task 2

This task is to implement the function ***Y = (A or B) and (C or D)*** in task2.vhd. Make sure to read the instructions before starting.

1. Add the task2.vhd file:
    a. Under “Flow Navigator” click “Add sources.”
    b. Select “Create or add design sources.”
    c. Add task2.vhd and then click “Finish.”
2. Once you have your vhdl source file, edit it to implement the function.
3. Make sure it’s syntax error free and can be synthesized.
4. Add the task2_tb.vhd file:
    a. Under “Flow Navigator” click “Add sources.”
    b. Select “Create or add simulation sources.”
    c. Add task2_tb.vhd.
    d. Make sure simulation set is “sim_2.”
    e. Click “Finish.
5. Select the right simulation set:
    a. Under “Flow Navigator” click “Simulation Settings.”
    b. Under “Simulation set” input “sim_2.”
    c. Under “Simulation top module name” input “task2_tb.”
    d. Click “Ok.”
6. Run the simulation and check your results. The expected output is on the last page of the assignment.
7. Vivado doesn’t include a way to print test bench results so you will have to take a screenshot.

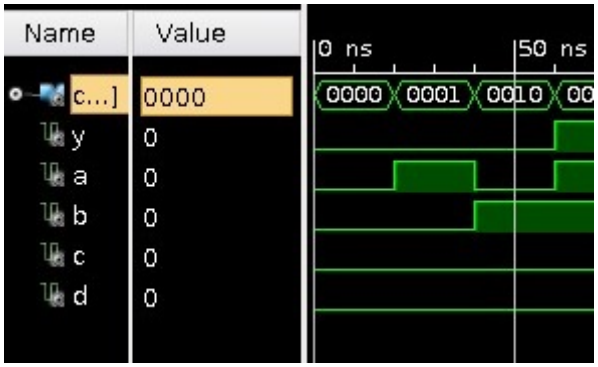
Turn in

Make sure everything is in a single PDF on Moodle. You can join PDFs with Adobe Acrobat if you have multiple PDFs. Name the assignment CAD1-xxxxxx-yyyyyy, where xxxxxx is the last name of one lab partner and yyyyyy is the last name of the other lab partner. Turn in only one pdf under one of the lab partner’s Moodle account.

Grading

Printout of task1.vhd	/3 Points
Printout of task2.vhd	/5 Points
Printout of task2 simulation results	/5 Points
Printout of task2 simulation results	/7 Points
	/Total of 20 Points

First part of waveform of Task1



First part of waveform of Task2