UNCC, Department of Electrical and Computer Engineering, ECGR 4101/5101
Fall 2005, Homework #8, Due: 11/7/05, at the beginning of class (20 points)

0. How long did this homework take you? (1 point)
1. Read the Russell Massey article "Introduction to Interrupts." In four lines of correct English, summarize Mr. Massey's article. (3 points)
2. Read the Jack Ganssle article "Interrupt Latency." In four lines of correct English, summarize the general objective of the article. (4 points)
3. How far apart in time can two interrupts be yet still be considered simultaneous if an M16C26 processor's clock is 8 MHz? SHOW YOUR WORK. (2 point)
4. For the M16C/262, list the following interrupts in order of decreasing priority: single-step, NMI, watchdog timer, reset, ADC conversion complete, UART0, receive UART2 transmit, Timer B2. (2 point)
5. Assume an enabled interrupt has occurred. Fill in the contents of the stack and update the registers listed when the processor is about to begin executing the ISR at address 0x0ff440. Recall that the FLG register is modified when the processor responds to an interrupt. Assume the following processor state immediately before the interrupt occurred. (8 points)
    - SP = 0x800,
    - PC = 0xff312
    - FLG = 0x3062
    - Stack contents as shown in table below.

Address	Value
0x07f9	
0x07fa	
0x07fb	
0x07fc	
0x07fd	
0x07fe	
0x07ff	
0x0800	
0x0801	

Register	Initial Value	Final Value
SP	0x0800	
PC	0x0ff312	
FLG	0x3062	