UNCC, Department of Electrical and Computer Engineering
ECGR4101/5101, Fall 2007, Homework #7, Due: 10/29/07, at the beginning of class (20 points)

0. (1 point) How long did this homework take you?
1. (3 points) Read the Stuart Ball article "Introduction to Interrupt Debugging." In four lines of correct English, summarize Mr. Ball's article.
2. (2 point) How far apart in time can two interrupts be yet still be considered simultaneous if an M16C62P processor's clock is 30 MHz? SHOW YOUR WORK.
3. (2 point) For the M16C/262, list the following interrupts in order of decreasing priority: single-step, NMI, watchdog timer, reset, ADC conversion complete, UART1transmit, Timer B2.
4. (9 points) Assume an enabled interrupt has occurred. Fill in the contents of the stack and update the registers listed when the processor is about to begin executing the ISR at address 0x0fa540. Recall that the FLG register is modified when the processor responds to an interrupt. Assume the following processor state immediately before the interrupt occurred.
    a. SP = 0x700,
    b. PC = 0xfa412
    c. FLG = 0x3062
    d. Stack contents as shown in table below.

Address	Value
0x06f9	
0x06fa	
0x06fb	
0x06fc	
0x06fd	
0x06fe	
0x06ff	
0x0700	
0x0701	

Register	Initial Value	Final Value
SP	0x0700	
PC	0x0fa412	
FLG	0x3062	

5. (3 point) Correct the three problems with the following interrupt service routine declaration.

```
#pragma new_isr INTERRUPT
int new_isr(int n) {
...
}
```