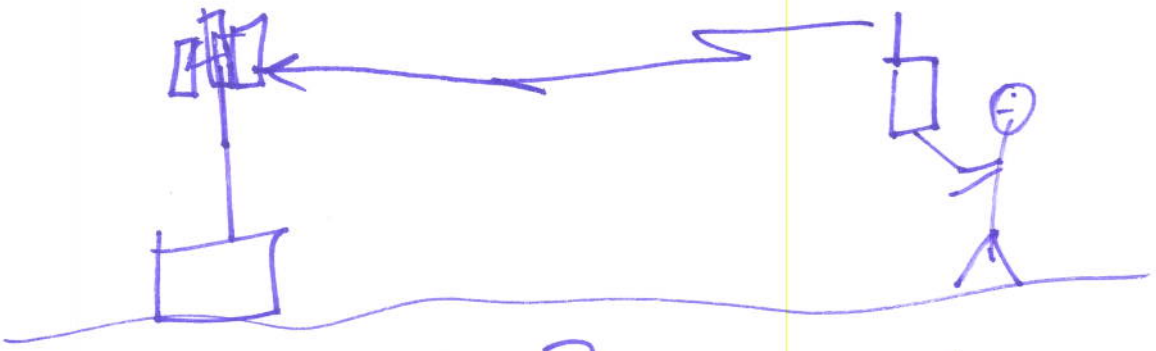
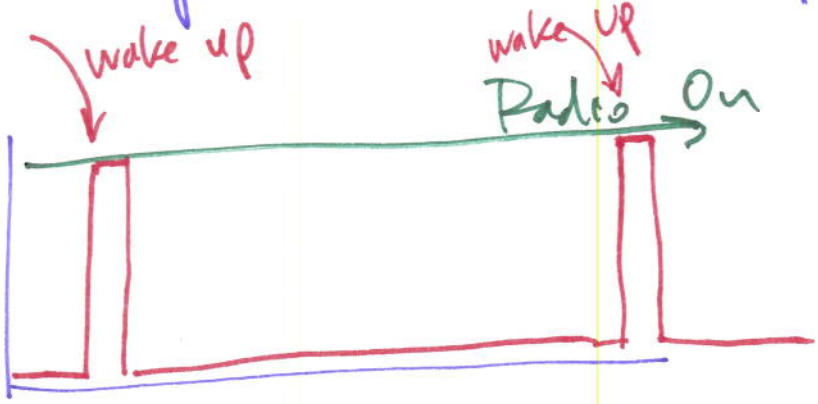
Embedded System Lecture 18



Run active? → draining batteries

Sleep? → "sipping" batteries

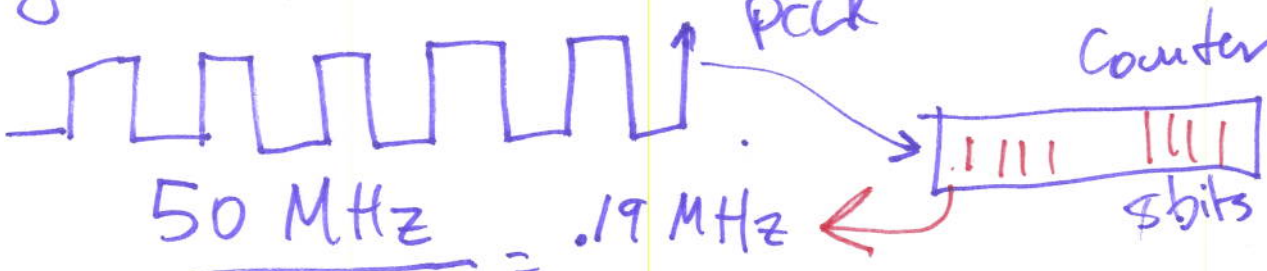


CDMA → 1.024 seconds → phone listen

Verizon

→ 2.048 seconds

Digital System → clock heart beat



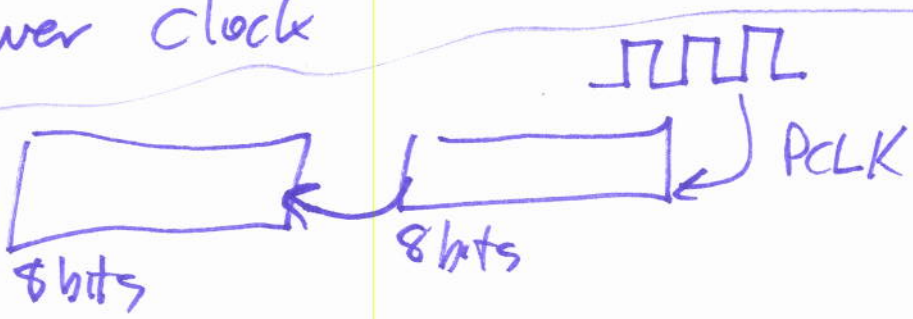
$$\frac{50\ \text{MHz}}{256} = .19\ \text{MHz}$$

Embedded Systems Lecture 18

How do we get closer to a (2)
1.024 ~~Hz~~ second period

1) Bigger counter
2) Slower clock

1) 16 bits



$$\frac{50\ \text{MHz}}{2^{16}} = 762.94\ \text{Hz}$$

2) Exercise: Tell me the best

a) PCLK
b) "value" of 16 bit register

to get 1.024 clock

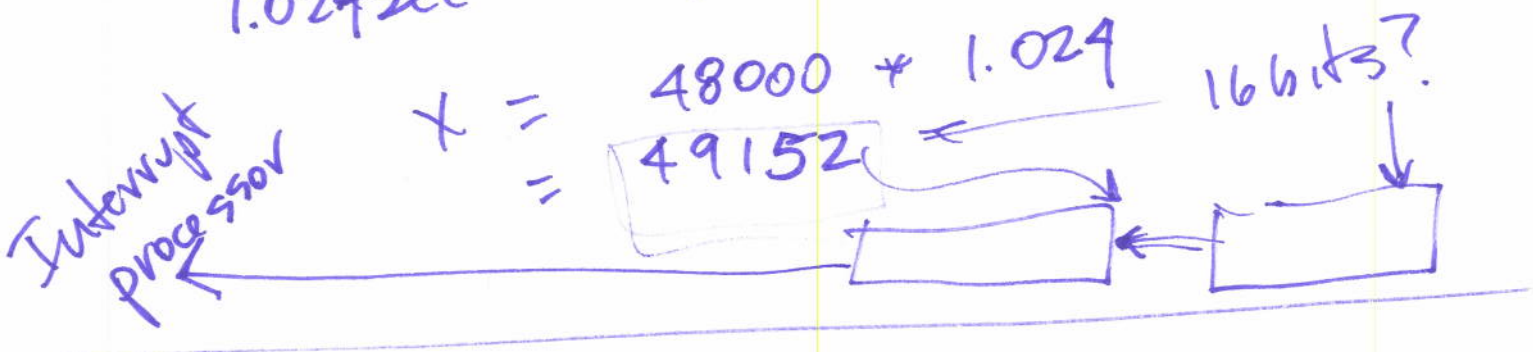
Divide my clock by 1024

$$\frac{50\ \text{MHz}}{1024} = 48\ \text{kHz} = 48000$$

PCLK
TCLK

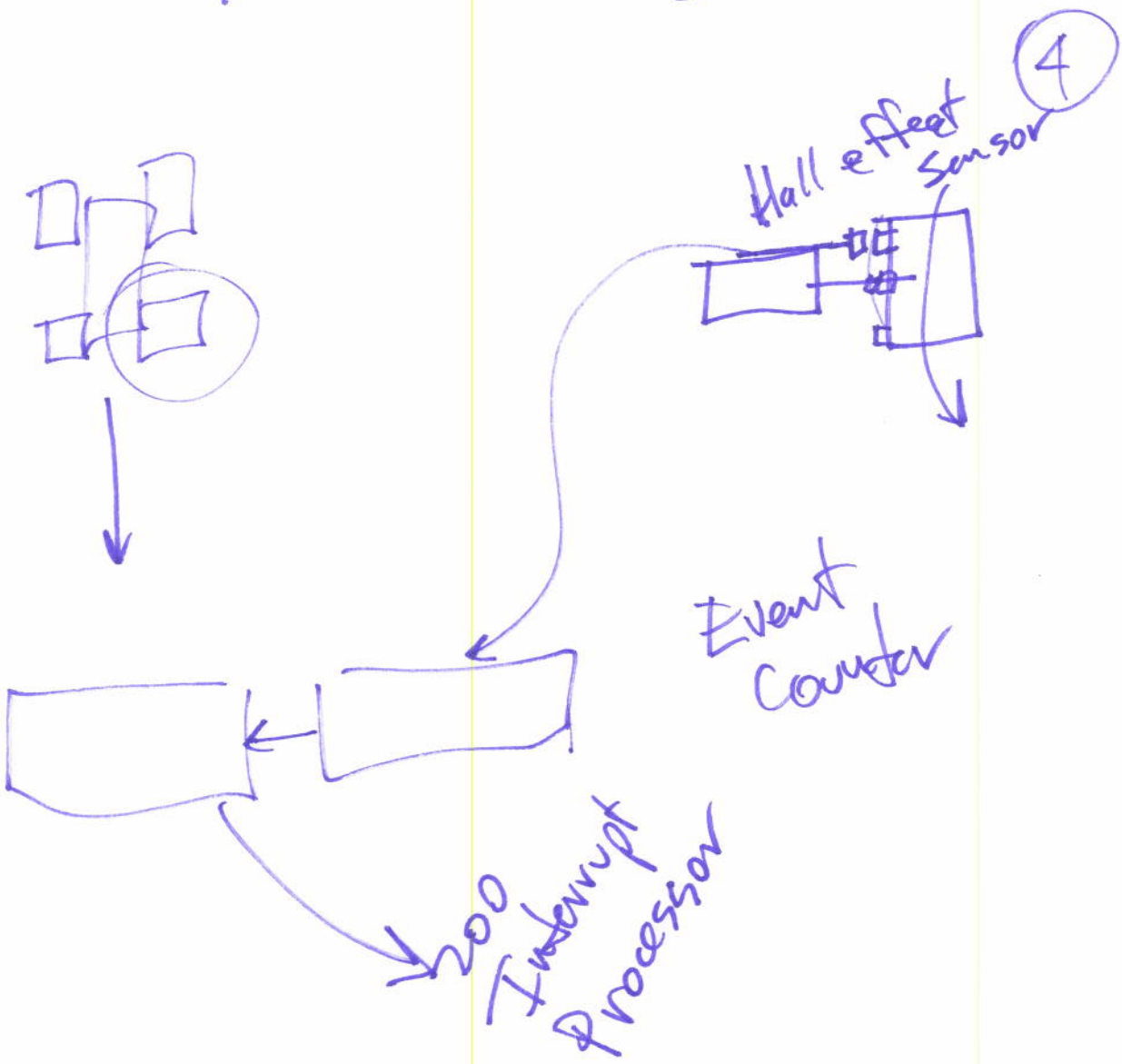
$$\frac{1}{1.024\text{sec}} = \frac{48000\ \text{Hz}}{X}$$

$$X = 48000 * 1.024$$
$$= 49152$$



50 MHz Clock

Divider	
2	25 MHz
4	12.5 MHz
8	
16	
⋮	
1024	
2048	
4096	
8192	6000 Hz

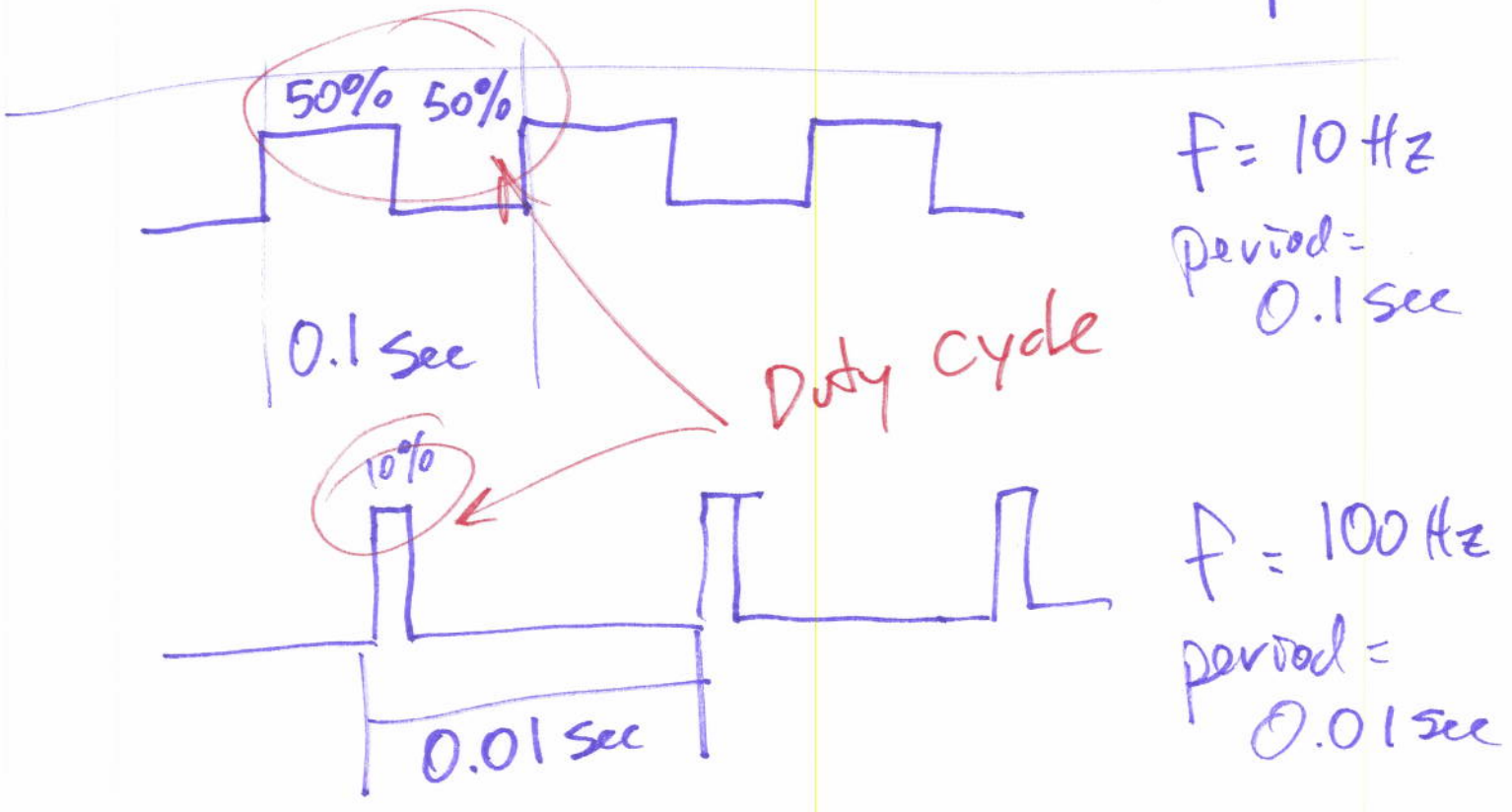

4
Hall effect Sensor
Event Counter
100 Interrupt Processor

Preset register: 49152

Set the clock → i.e. PCLK / ~~1024~~

Set up how the ~~clock~~ Timer will run

* start / stop
* registers – cascade (which ones)
  (how to feed)
* which input (external event?)
* out put → interrupting signal
  → send off chip



Embedded App of Day

Whirlpool Oven Model _____

- Mechanical enclosure
- Electrical connection
- Electronic Board - Assembled
  - PCB
  - LCD
  - Resistors
  - Caps
  - Assembled Processor
    - Processor
    - Software

UNC Charlotte, Department of Electrical and Computer Engineering
ECGR 4101/5101, Fall 2012, Quiz #14

Your name: Solution Show all work

Modify the following code to set up a 1KHz square wave with a 50% duty cycle.

```
7.  void InitTimer(void){
8.      MSTP(TMR0) = 0;    //Activate TMR0 unit   MSTP(TMR1) = 0;
9.      TMR0.TCCR.BIT.CSS = 1;    //Count source is PCLK/8
10.     TMR0.TCCR.BIT.CKS = 2;    TMR0.TCCR.BIT.CSS = 3;
11.     TMR0.TCR.BIT.CCLR = 1;    //Timer resets at compare match A
12.     TMR0.TCSR.BIT.OSA = 2;    //1-output at compare match A
13.     TMR0.TCSR.BIT.OSB = 1;    //0-output at compare match B
14.     TMR0.TCORA = 0x55;0B //Frequency   TMR1.TCORA = 0xB8;
15.     TMR0.TCORB = 0x20;05 //Duty cycle   TMR1.TCORB = 0xDC;
16.     //Pulse outputs to TMo0, which is also P22/USB_DRPD
17.     //Can be monitored by touching a scope probe to the top
18.     //of resistor R46, near bottom right corner of ethernet
19.     //port. Port JN2 provides a ground.
20. }
```

TCORA = 1kHz
TCORB = 1/2 of TCORA value

$$\frac{1}{24\ \text{MHz (PCLK)}} * \frac{n\ (\text{clock Div})}{1} * \frac{m\ (\text{counts})}{1} = 0.001\ \text{sec}$$

n	m↓
1	24000
2	12000
8	3000
32	750
64	375
128	187.5
1024	

Test Question - If you set it as this how far do you go?

	TMR0	TMR1
TCORA	0x0B	0xB8
TCORB	0x05	0xDC