Serial Communications

Lecture 11

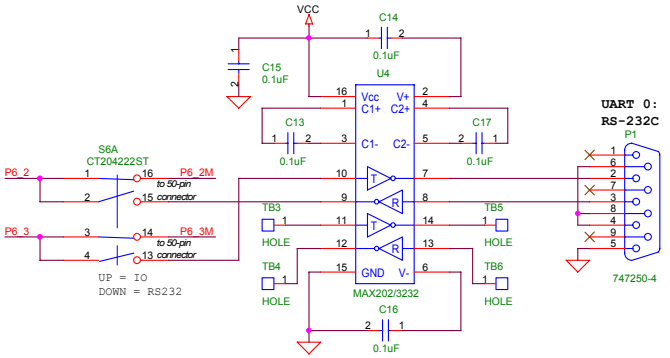
In these notes . . .

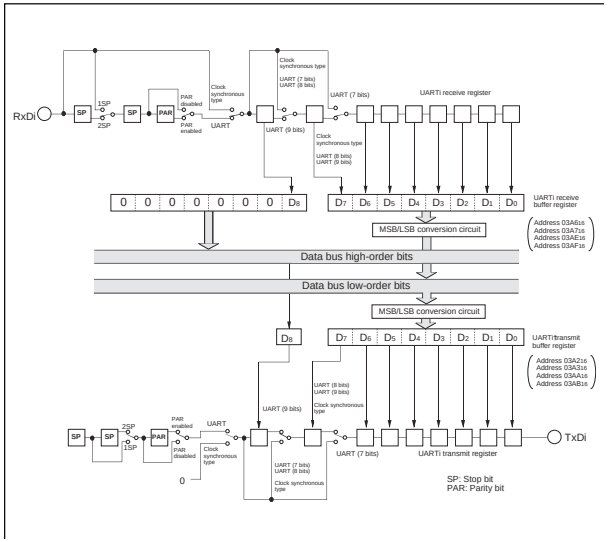
General Communications

Serial Communications

- RS232 standard
- UART operation
- Polled Code
- Interrupt Driven Code

Read M16C/62 Hardware Manual pp. 137-182





Data Communications

There was no standard for networks in the early days and as a result it was difficult for networks to communicate with each other.

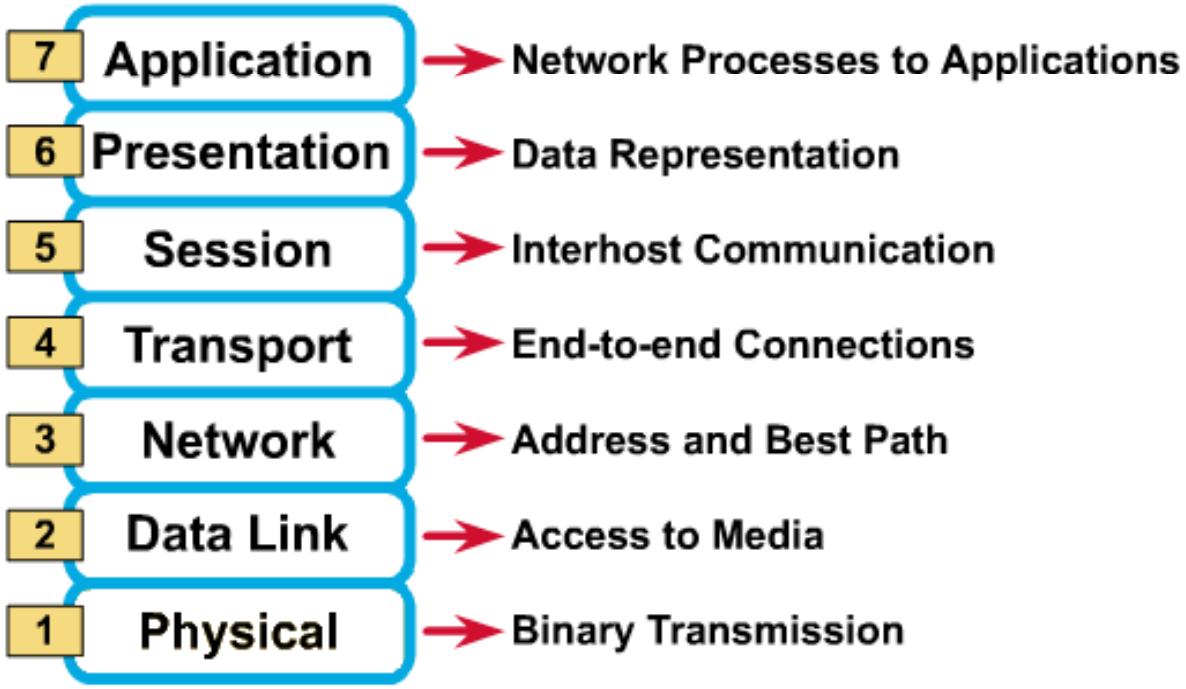
The International Organization for Standardization (ISO) recognized this and in 1984 introduced the Open Systems Interconnection (OSI) reference model.

The OSI reference model organizes network functions into seven numbered layers.

Each layer provides a service to the layer above it in the protocol specification and communicates with the same layer's software or hardware on other computers.

Layers 5-7 are concerned with services for the applications.

Layers 1-4 are concerned with the flow of data from end to end through the network



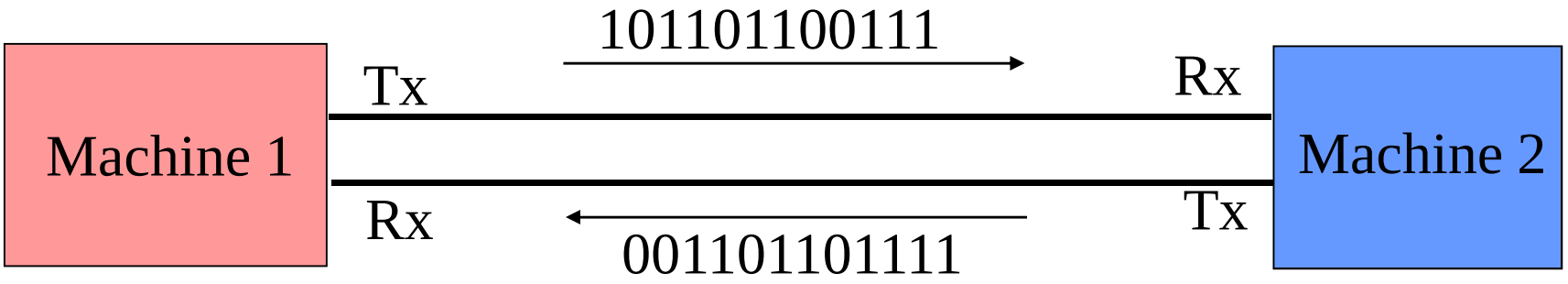
Physical Layer (1) – Serial Communications

The basic premise of serial communications is that one or two wires are used to transmit digital data.

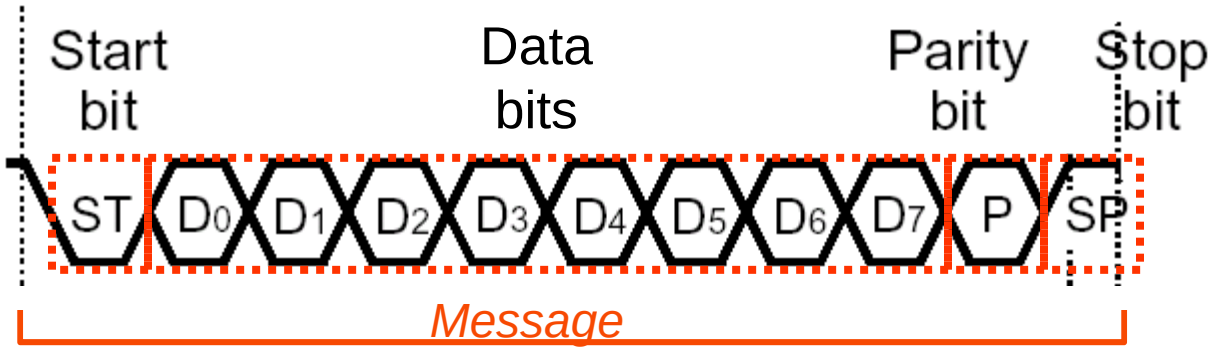
- Of course, ground reference is also needed (extra wire)

Can be one way or two way, usually two way, hence two communications wires.

Often other wires are used for other aspects of the communications (ground, “clear-to-send”, “data terminal ready”, etc).



Serial Communication Basics



Send one bit of the message at a time

Message fields

- Start bit (one bit)
- Data (LSB first or MSB, and size – 7, 8, 9 bits)
- Optional parity bit is used to make total number of ones in data even or odd
- Stop bit (one or two bits)

All devices on network or link must use same communications parameters

- The speed of communication must be the same as well (300, 600, 1200, 2400, 9600, 14400, 19200, etc.)

More sophisticated network protocols have more information in each message

- Medium access control – when multiple nodes are on bus, they must arbitrate for permission to transmit
- Addressing information – for which node is this message intended?
- Larger data payload
- Stronger error detection or error correction information
- Request for immediate response (“in-frame”)

Bit Rate vs. Baud Rate

Bit Rate: how many ***data bits*** are transmitted per second?

Baud Rate: how many ***symbols*** are transmitted per second?

- == How many times does the communication channel change state per second?
- A symbol may be represented by a voltage level, a sine wave's frequency or phase, etc.

These may be different

- Extra symbols (channel changes) may be inserted for framing, error detection, acknowledgment, etc. These ***reduce*** the bit rate
- A single symbol might encode more than one bit. This ***increases*** the bit rate.
  - E.g. multilevel signaling, quadrature amplitude modulation, phase amplitude modulation, etc.

Serial Communication Basics

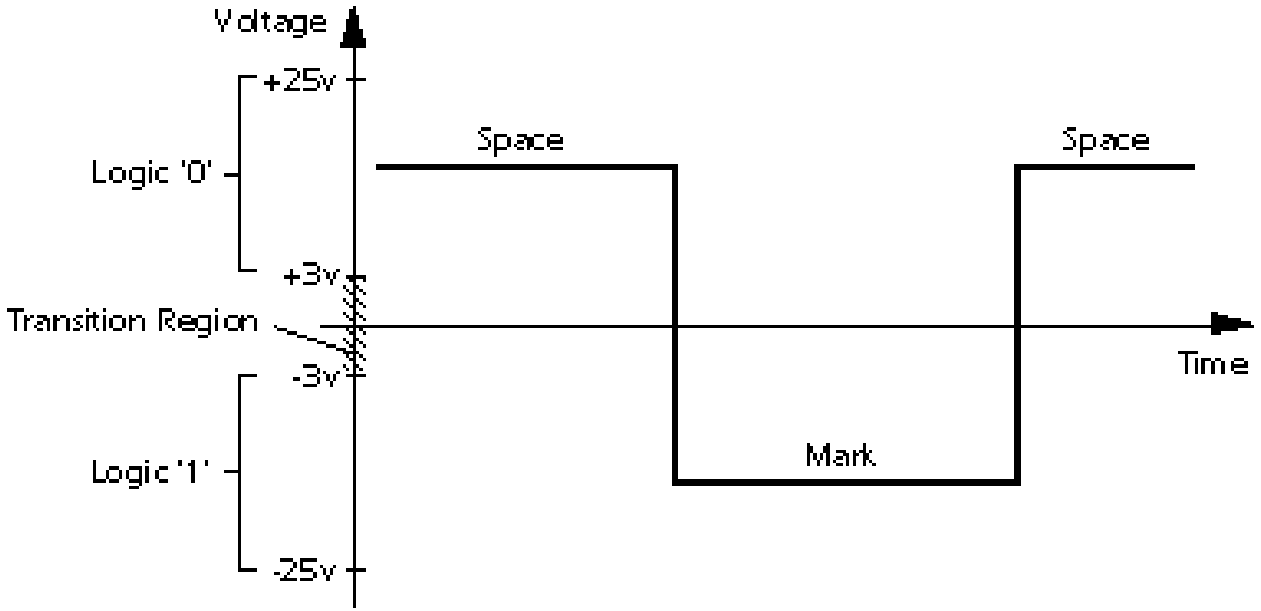
RS232: rules on connector, signals/pins, voltage levels, handshaking, etc.

RS232: Fulfilling All Your Communication Needs, Robert Ashby

Quick Reference for RS485, RS422, RS232 and RS423

Not so quick reference:
The RS232 Standard: A Tutorial with Signal Names and Definitions,
Christopher E. Strangio

Bit vs Baud rates:
http://www.totse.com/en/technology/telecommunications/bits.html



UART Concepts

UART

- Universal – configurable to fit protocol requirements
- Asynchronous – no clock line needed to deserialize bits
- Receiver/Transmitter

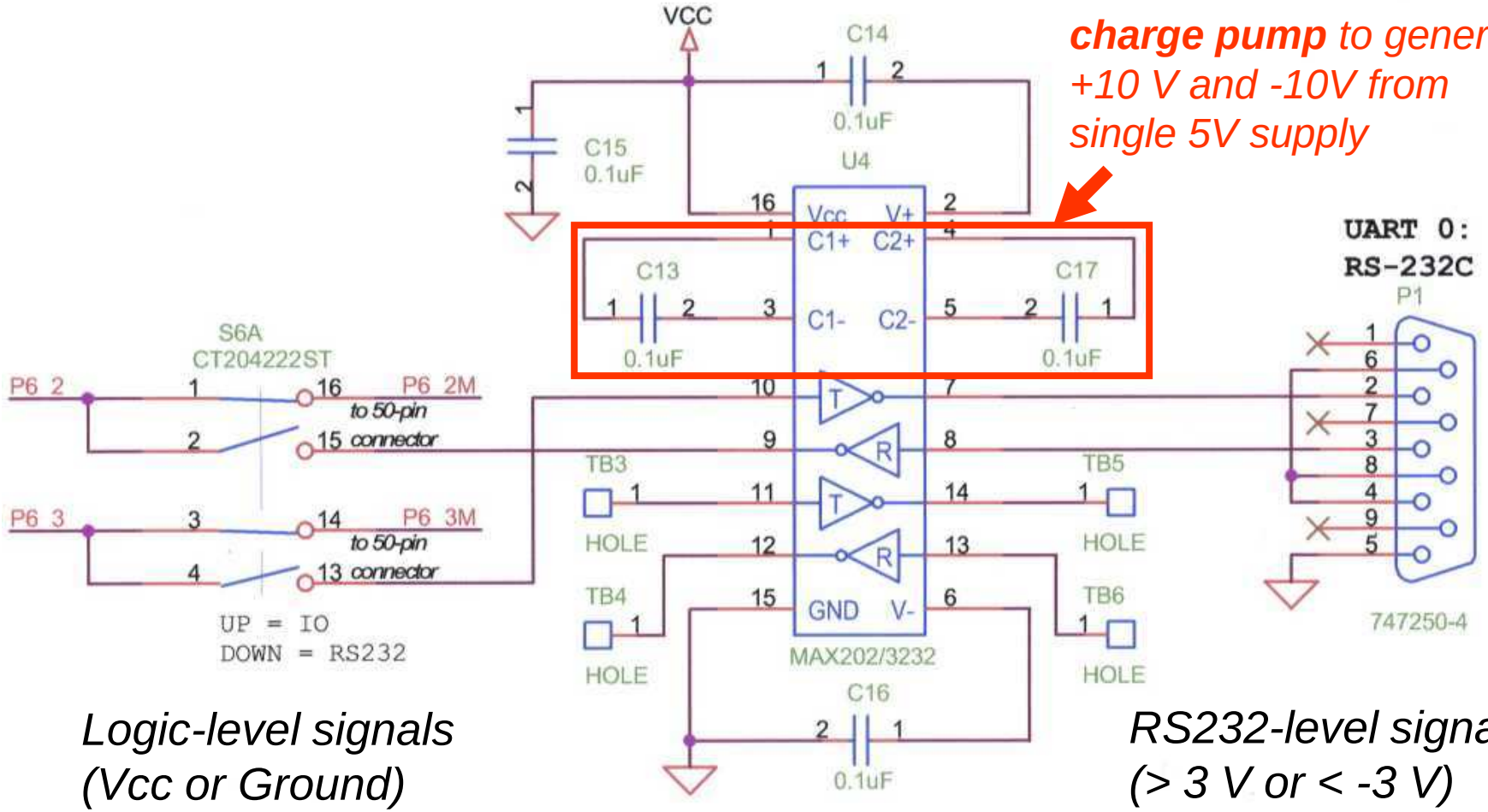
M30626 has three

- UART0, 1, and 2
- UART1 talks to USBMon board, enables us to do in-circuit debugging
- Can operate in asynchronous or synchronous (not used here) modes
- See MCU Hardware Manual for details, or else the remaining slides might be confusing

RS232 Communications Circuit

Example RS-232 buffer (level-shifting) circuit

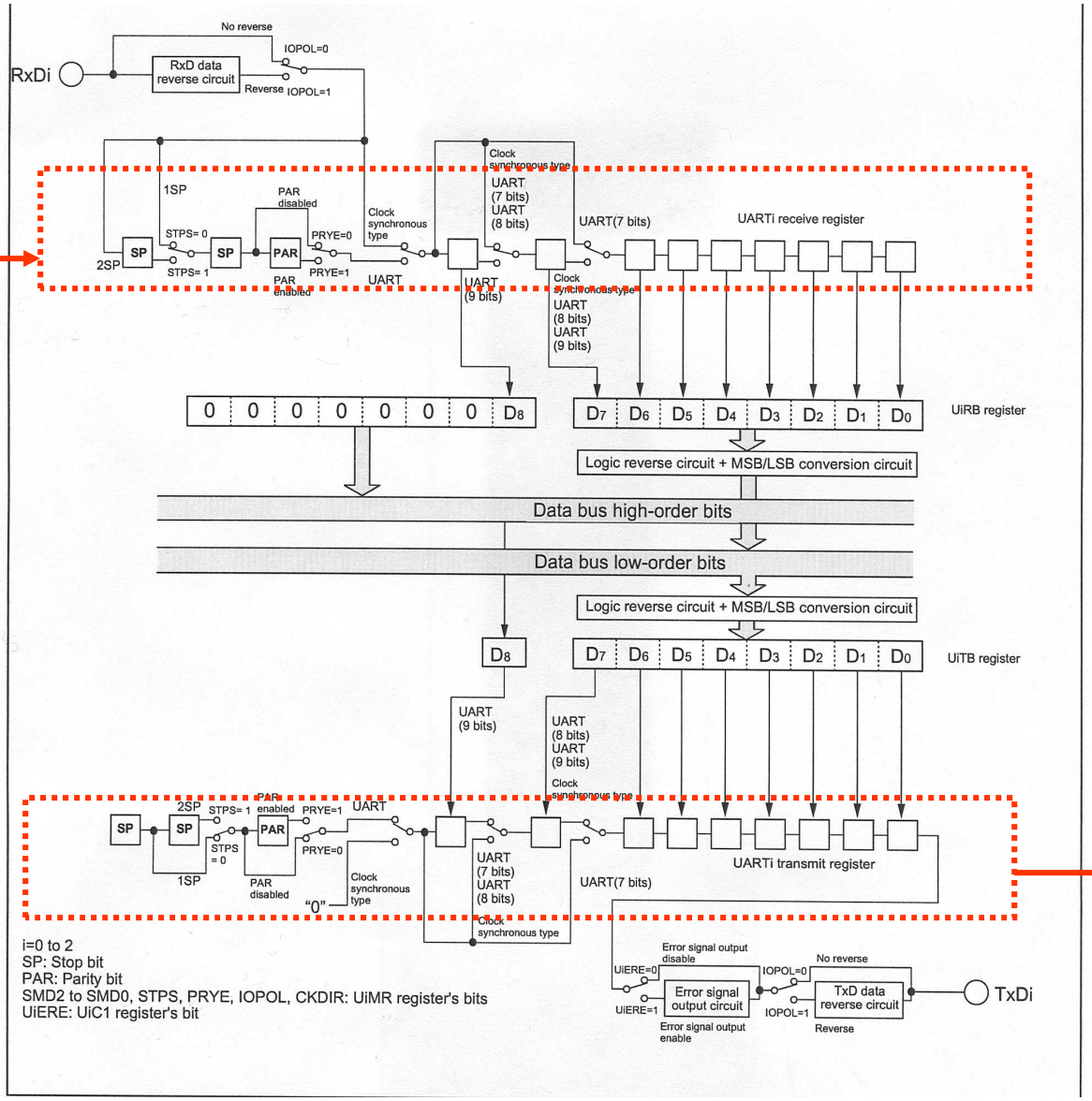
- Not included on SKP16C62



UART Concepts

UART subsystems

- –Two fancy shift registers
  - Parallel to serial for transmit
  - Serial to parallel for receive
- –Programmable clock source
  - Clock must run at 16x desired bit rate
- –Error detection
  - Detect bad stop or parity bits
  - Detect receive buffer overwrite
- –Interrupt generators
  - Character received
  - Character transmitted, ready to send another



Setting up the Serial Port

We will use UART 0, so all of the references to a UART will have “u0” in them.

There are several “control” registers you need to set up before you can communicate.

- First, you need to set up the speed of your port.
- Select 8 data bits, no parity, one stop bit (8N1)
- Enable transmitter and receiver

Code examples:

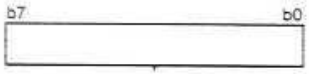
- main_uart.c/skp_bsp.h in the SKPTest application
- serial_poll_demo.c/serial_poll_includes on notes page

Setting up Speed of the Serial Port

Baud rate = 19,200 baud

- 12 MHz/(16*19,200 baud) = 39.1
- Load u0brg with 39-1 = 38
- Actual baud rate = 12 MHz/(16*39) = 19230.8 baud
  = 0.16% error
- If error is too large, communication fails
- This uses count source f1. You can also select f8 (1/8 clock) and f32 (1/32 of clock). Adjust BRG accordingly.

UARTi bit rate generator (Note 1, 2)



Symbol	Address	When reset
U0BRG	$03A1_{16}$	Indeterminate
U1BRG	$03A9_{16}$	Indeterminate
U2BRG	0379_{16}	Indeterminate

Function	Values that can be set	R	W
Assuming that set value = n, BRGi divides the count source by n + 1	00_{16} to FF_{16}	X	O

Note 1: Write a value to this register while transmit/receive halts.
Note 2: Use MOV instruction to write to this register.

Example – Change to Slower Clock

Baud rate = 300 baud

- 12 MHz/(16*300 baud) = 2500
- Load u0brg with 2500-1 = 2499
- u0brg max value is 256! This will not work!

Baud rate = 300 baud, 1/32 clock

- 12 MHz * 1/32 clock/(16*300 baud) = 78.125
- Load u0brg with 78-1 = 77
- Actual baud rate = 12 MHz * 1/32 clock /(16*78) = 300.5 baud
  = 0.17% error
- If error is too large, communication fails

Example – Bad BRG selection

Baud rate = 19200 baud, 1/32 clock

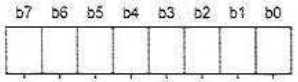
- 12 MHz * 1/32 clock/(16*19200 baud) = 1.2
- Set brg with 0!

Baud rate = 19200 baud, 1/8 clock

- 12 MHz * 1/8 clock/(16*19200 baud) = 4.9
- Load u0brg with 4-1=3
- Actual baud rate = 12 MHz * 1/32 clock /(16*4) = 23437.5 baud
  = 22.1% error
- Error is too large, communication will fail

UART0 Control Register 0

UARTi transmit/receive control register 0



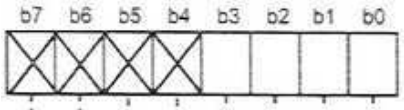
Symbol: UiC0(i=0,1) | Address: 03A4₁₆, 03AC₁₆ | When reset: 08₁₆

Bit symbol	Bit name	Function (During clock synchronous serial I/O mode)	Function (During UART mode)	R	W
CLK0	BRG count source select bit	b1 b0 0 0 : f1 is selected 0 1 : f8 is selected 1 0 : f32 is selected 1 1 : Inhibited	b1 b0 0 0 : f1 is selected 0 1 : f8 is selected 1 0 : f32 is selected 1 1 : Inhibited	○	○
CLK1				○	○
CRS	$\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function select bit	Valid when bit 4 = "0" 0 : $\overline{\text{CTS}}$ function is selected (Note 1) 1 : $\overline{\text{RTS}}$ function is selected (Note 2)	Valid when bit 4 = "0" 0 : $\overline{\text{CTS}}$ function is selected (Note 1) 1 : $\overline{\text{RTS}}$ function is selected (Note 2)	○	○
TXEPT	Transmit register empty flag	0 : Data present in transmit register (during transmission) 1 : No data present in transmit register (transmission completed)	0 : Data present in transmit register (during transmission) 1 : No data present in transmit register (transmission completed)	○	×
CRD	$\overline{\text{CTS}}$/$\overline{\text{RTS}}$ disable bit	0 : $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function enabled 1 : $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled (P6₀ and P6₄ function as programmable I/O port)	0 : $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function enabled 1 : $\overline{\text{CTS}}$/$\overline{\text{RTS}}$ function disabled (P6₀ and P6₄ function as programmable I/O port)	○	○
NCH	Data output select bit	0 : TXDi pin is CMOS output 1 : TXDi pin is N-channel open-drain output	0: TXDi pin is CMOS output 1: TXDi pin is N-channel open-drain output	○	○
CKPOL	CLK polarity select bit	0 : Transmit data is output at falling edge of transfer clock and receive data is input at rising edge 1 : Transmit data is output at rising edge of transfer clock and receive data is input at falling edge	Must always be "0"	○	○
UFORM	Transfer format select bit	0 : LSB first 1 : MSB first	Must always be "0"	○	○

Note 1: Set the corresponding port direction register to "0".
Note 2: The settings of the corresponding port register and port direction register are invalid.

UART0 Control Register 1

UARTi transmit/receive control register 1 (i=0, 1)

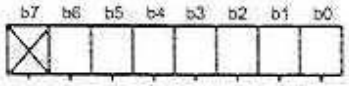


Symbol	Address	When reset
UiC1(i=0,1)	$03A5_{16}$,$03AD_{16}$	02_{16}

Bit symbol	Bit name	Function (During clock synchronous serial I/O mode)	Function (During UART mode)	R	W
TE	Transmit enable bit	0 : Transmission disabled 1 : Transmission enabled	0 : Transmission disabled 1 : Transmission enabled	○	○
TI	Transmit buffer empty flag	0 : Data present in transmit buffer register 1 : No data present in transmit buffer register	0 : Data present in transmit buffer register 1 : No data present in transmit buffer register	○	×
RE	Receive enable bit	0 : Reception disabled 1 : Reception enabled	0 : Reception disabled 1 : Reception enabled	○	○
RI	Receive complete flag	0 : No data present in receive buffer register 1 : Data present in receive buffer register	0 : No data present in receive buffer register 1 : Data present in receive buffer register	○	×
Nothing is assigned. In an attempt to write to these bits, write 0 . The value, if read, turns out to be 0 .				—	—

UART Control Register 2

UART transmit/receive control register 2



Symbol: UCON | Address: 03B0₁₆ | When reset: X0000000₂

Bit symbol	Bit name	Function (During clock synchronous serial I/O mode)	Function (During UART mode)	R	W
U0IRS	UART0 transmit interrupt cause select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	O	O
U1IRS	UART1 transmit interrupt cause select bit	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	0 : Transmit buffer empty (TI = 1) 1 : Transmission completed (TXEPT = 1)	O	O
U0RRM	UART0 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enable	Must always be 0	O	O
U1RRM	UART1 continuous receive mode enable bit	0 : Continuous receive mode disabled 1 : Continuous receive mode enabled	Must always be 0	O	O
CLKMD0	CLK/CLKS select bit 0	Valid when bit 5 = 1 0 : Clock output to CLK1 1 : Clock output to CLKS1	Invalid	O	O
CLKMD1	CLK/CLKS select bit 1 (Note)	0 : Normal mode (CLK output is CLK1 only) 1 : Transfer clock output from multiple pins function selected	Must always be 0	O	O
RCSP	Separate $\overline{\text{CTS}}/\overline{\text{RTS}}$ bit	0 : $\overline{\text{CTS}}/\overline{\text{RTS}}$ shared pin 1 : $\overline{\text{CTS}}/\overline{\text{RTS}}$ separated	0 : $\overline{\text{CTS}}/\overline{\text{RTS}}$ shared pin 1 : $\overline{\text{CTS}}/\overline{\text{RTS}}$ separated	O	O
Nothing is assigned. In an attempt to write to this bit, write 0 . The value, if read, turns out to be indeterminate.				—	—

Note: When using multiple pins to output the transfer clock, the following requirements must be met:
* UART1 internal/external clock select bit (bit 3 at address 03A8₁₆) = 0 .

UART0 Tx/Rx Mode Register

UARTi transmit/receive mode register

b7	b6	b5	b4	b3	b2	b1	b0
0							

Symbol: UiMR(i=0,1) — Address: 03A016, 03A816 — When reset: 0016

Bit symbol	Bit name	Function (During clock synchronous serial I/O mode)	Function (During UART mode)	R	W
SMD0	Serial I/O mode select bit	Must be fixed to 001	b2 b1 b0 1 0 0 : Transfer data 7 bits long 1 0 1 : Transfer data 8 bits long 1 1 0 : Transfer data 9 bits long	○	○
SMD1		b2 b1 b0 0 0 0 : Serial I/O invalid 0 1 0 : Inhibited 0 1 1 : Inhibited 1 1 1 : Inhibited	0 0 0 : Serial I/O invalid 0 1 0 : Inhibited 0 1 1 : Inhibited 1 1 1 : Inhibited	○	○
SMD2				○	○
CKDIR	Internal/external clock select bit	0 : Internal clock 1 : External clock	0 : Internal clock 1 : External clock (Note)	○	○
STPS	Stop bit length select bit	Invalid	0 : One stop bit 1 : Two stop bits	○	○
PRY	Odd/even parity select bit	Invalid	Valid when bit 6 = "1" 0 : Odd parity 1 : Even parity	○	○
PRYE	Parity enable bit	Invalid	0 : Parity disabled 1 : Parity enabled	○	○
Reserved		Must always be "0"		○	○

Note: Set the corresponding port direction register to 0.

Configuring UART0

```
void init_UART0() {
  // UART 0 bit rate generator
  u0brg =38;

  // UART 0 transmit/receive mode register
  smd2_u0mr = 1;   // eight data bits
  smd1_u0mr = 0;
  smd0_u0mr = 1;
  ckdir_u0mr = 0; // internal clock
  stps_u0mr = 0;
  pry_u0mr = 0;
  prye_u0mr = 0; // no parity

  // uart0 t/r control register 0
  // 12 MHz -> 19,200 baud
  clk1_u0c0 = 0; // select f/1 clock
  clk0_u0c0 = 0;
  nch_u0c0 = 0; // CMOS push-pull output
  ckpol_u0c0 = 0; // required
  uform_u0c0 = 0; // required
  crs_u0c0 = 0; // required
  crd_u0c0 = 1; // required

  // uart0 t/r control register 1
  te_u0c1 = 1; // enable transmitter
  re_u0c1 = 1; // enable receiver

  // uart t/r control register 2
  u0irs = 0;   // select interrupt source
  u1rrm = 0;   // select interrupt source
  clkmd0 = 0;  // n/a
  clkmd1 = 0;  // n/a
  rcsp=1;      // rxdo port to p6_2
}
```

Using the UART

When can we transmit?

- Transmit buffer must be empty
- Can poll `ti_u0c1` (UART0, control register 1, transmit buffer empty, 0x03A5, bit 1)
- Or we can use an interrupt, in which case we will need to queue up data

Put data to be sent into `u0tbl` (UART0, transmitter buffer, low byte, 0x03A2)

Notice the differences between ones (`1`) and ells (`l`)

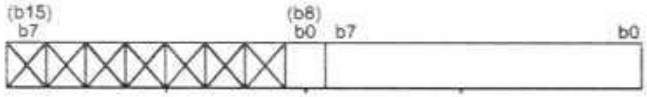
When can we receive a byte?

- Receive buffer must be full
- Can poll `ri_u0c1` (UART0, control register 1, receive complete flag, 0x03A5, bit 3)
- Or we can use an interrupt, and again we will need to queue the data

Get data from `u0rbl` (UART0, receive buffer, low byte, 0x03A6)

Transmit Buffer

UARTi transmit buffer register (Note)



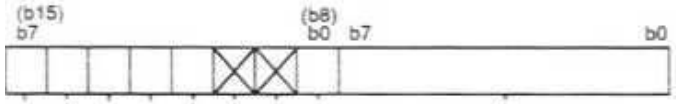
Symbol	Address	When reset
U0TB	$03A3_{16}$, $03A2_{16}$	Indeterminate
U1TB	$03AB_{16}$, $03AA_{16}$	Indeterminate
U2TB	$037B_{16}$, $037A_{16}$	Indeterminate

Function	R	W
Transmit data	X	O
Nothing is assigned. In an attempt to write to these bits, write 0 . The value, if read, turns out to be indeterminate.	–	–

Note: Use MOV instruction to write to this register.

Receive Buffer

UARTi receive buffer register



Symbol	Address	When reset
U0RB	$03A7_{16}$, $03A6_{16}$	Indeterminate
U1RB	$03AF_{16}$, $03AE_{16}$	Indeterminate
U2RB	$037F_{16}$, $037E_{16}$	Indeterminate

Bit symbol	Bit name	Function (During clock synchronous serial I/O mode)	Function (During UART mode)	R	W
—	———	Receive data	Receive data	○	×
Nothing is assigned. In an attempt to write to these bits, write 0 . The value, if read, turns out to be 0 .				—	—
ABT	Arbitration lost detecting flag (Note 2)	0 : Not detected 1 : Detected	Invalid	○	○
OER	Overrun error flag (Note 1)	0 : No overrun error 1 : Overrun error found	0 : No overrun error 1 : Overrun error found	○	×
FER	Framing error flag (Note 1)	Invalid	0 : No framing error 1 : Framing error found	○	×
PER	Parity error flag (Note 1)	Invalid	0 : No parity error 1 : Parity error found	○	×
SUM	Error sum flag (Note 1)	Invalid	0 : No error 1 : Error found	○	×

Note 1: Bits 15 through 12 are set to 0 when the serial I/O mode select bit (bits 2 to 0 at addresses $03A0_{16}$, $03A8_{16}$ and 0378_{16}) are set to 000_2 or the receive enable bit is set to 0 .
(Bit 15 is set to 0 when bits 14 to 12 all are set to 0 .) Bits 14 and 13 are also set to 0 when the lower byte of the UARTi receive buffer register (addresses $03A6_{16}$, $03AE_{16}$ and $037E_{16}$) is read out.
Note 2: Arbitration lost detecting flag is allocated to U2RB and only "0" must be written. Nothing is assigned in bit 11 of U0RB and U1RB. Set to "0" when writing. If read, value is "0".

Example 1: Send Out Many Characters

Send out every character and symbol from ‘A’ to ‘z’ and then repeat

Use polling to determine when transmit buffer is empty and can be reloaded

```
void demo1() {
  // polled transmit demo
  unsigned long ctr;
  char c='A';
  while (SW1) {
    while (!ti_u0c1); // wait for
                      // transmit buffer empty
    for (ctr=0; ctr<50000; ctr++);
                      // delay so the letters
                      // come out slowly
    u0tbl = c; // load c into
                      // transmit buffer
    c++; // !
    if (c>'z')
      c = 'A'; // wrap around
  }
}
```

Example 2: Make the Code More Elegant

Create a function to transmit a null-terminated string

```
void demo2_ser_tx(far char * buf) {
  // polled buffer transmit demo
  // transmit a null-terminated
  // string
  while (*buf) {
    while (!ti_u0c1); // wait for
              // transmitter empty
    u0tbl = *buf; // load
              // character into buffer
    buf++; // increment buffer
              // pointer
  }
}
void demo2() {
  while (SW1) {
    demo2_ser_tx("Testing!\n\r");
    delay(100000);
  }
}
```

Example 3: Echo Received Data

- Wait for character to be received (via polling)
- Add one to character if switch 2 is pressed (LSSC (laughably simple substitution cipher))
- Wait for transmitter to be empty (ready)
- Send character
- If the character is a “return” send a line feed to make terminal scroll to new line

```
void demo3() {
  //  polling echo example
  char c;
  while (SW1) {
    while (!ri_u0c1) // await rx
      ;
    c = u0rbl; // get character
    if (!SW2) // "Encrypt“ c
      c += 1;
    while (!ti_u0c1) // await tx
      ;
    u0tbl = c; // send character
    // cr/lf translation for terminal
    if (c == '\r') {
      while (!ti_u0c1)
                ;
      u0tbl = '\n';
    }
  }
}
```