



JTAG

(JOINT TEST ACTION GROUP)

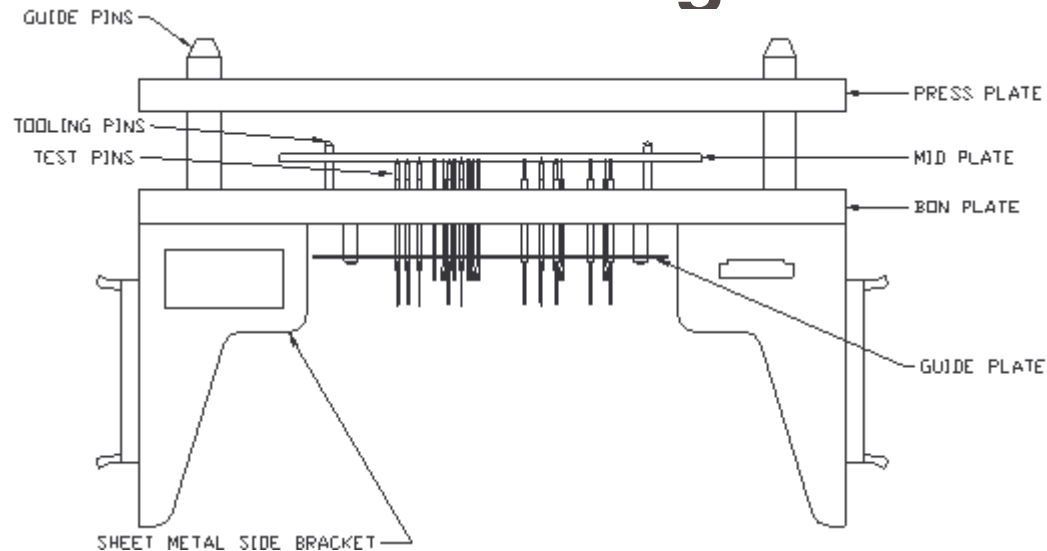
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Topics Discussed....

- n BED OF NAILS(BON TESTER)
- n What is JTAG ???
- n Advantages
- n Boundary Scan logic and Architecture
- n Real JTAG Applications

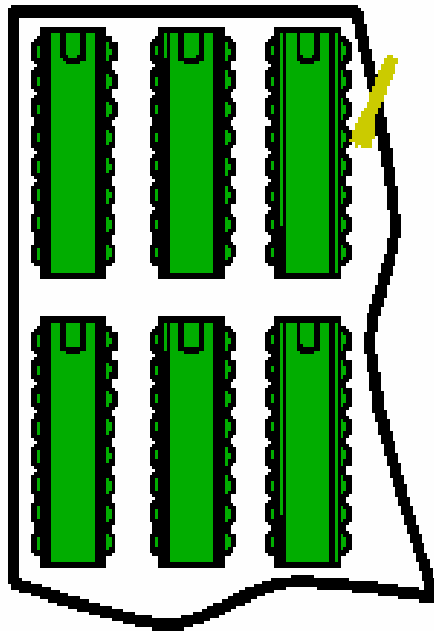
BED OF NAILS FIXTURE

n PCB Testing was done using Bed of Nails in circuit testing

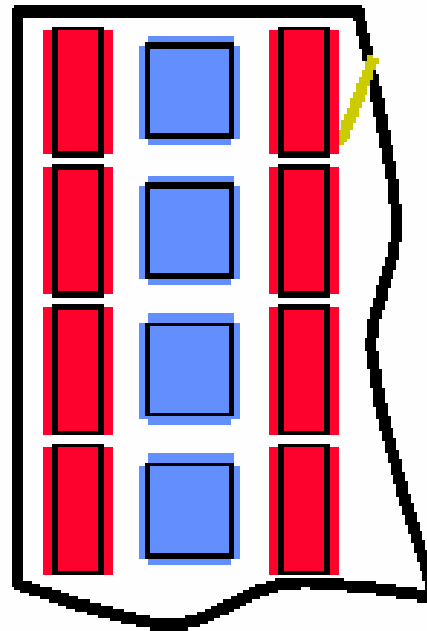


INCREASED PROBLEM OF TEST

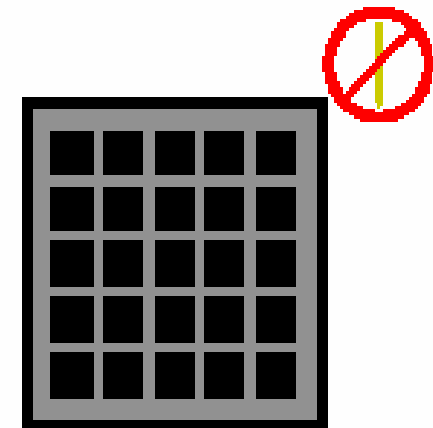
- Miniaturization results in loss of test access



Yesterday



Today

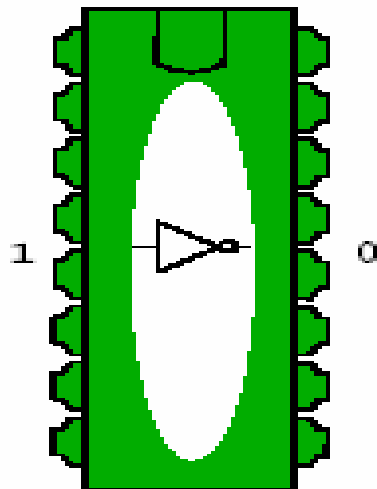


Tom orrow ?

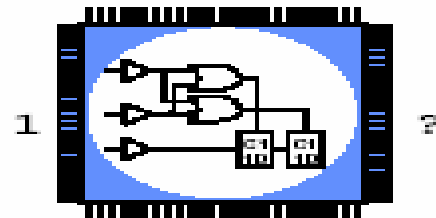
Circuit Complexity

The Ever-Expanding Chip

- Increasing integration at chip level complicates controllability



Yesterday



Today

DEVELOPMENT COST



Cost will increase by a factor of ten as fault finding moves from one level of complexity to the next. The result:

- *Reduced Profit Margins*
- *Delayed Product Introduction*
- *Dissatisfied Customers*

1. Device level	1 unit of cost
2. Board level	10 units of cost
3. System level	100 units of cost
4. Field level	1,000 units of cost

JTAG (1149.1 STANDARD)

IEEE 1149.1, a standard 4 wire serial protocol protocol that established the details of access to any chip with a JTAG port .

- n Boundary scan testing of Integrated Circuits(IC's) and boards.
- n Debug Embedded devices.
- n System level debug capability

What can it be used for?

The standard defines instructions that can be used to perform :

- n Functional Tests
- n Interconnect tests
- n Built-in self test procedures.

Advantages

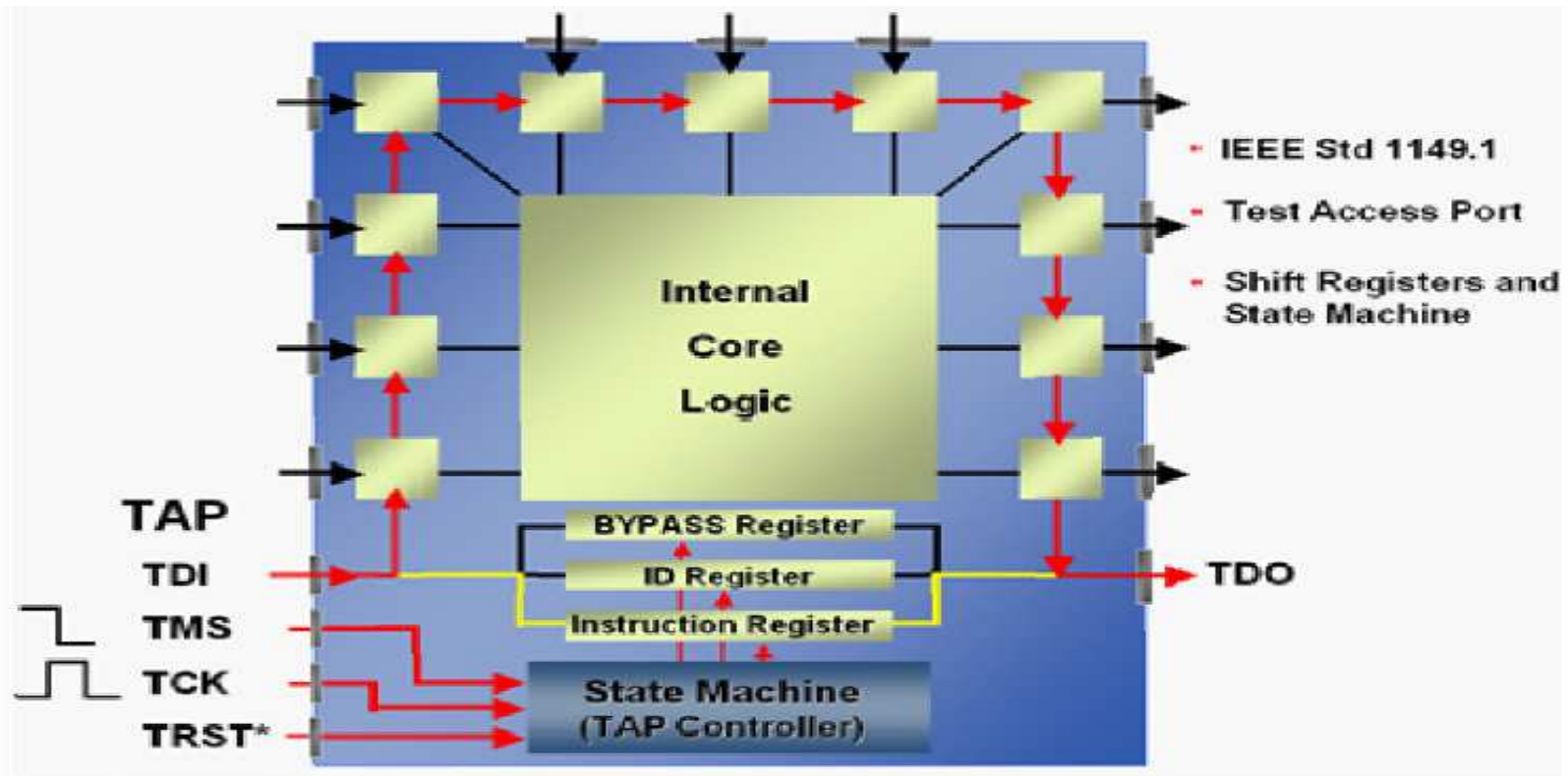
- n The need for physical test points on the board is eliminated leading to significant savings as a result of simpler board layouts.
- n Less costly test fixtures.
- n reduced time on in-circuit test systems.
- n increased use of standard interfaces.
- n faster time-to-market.

Boundary Scan

n What is Boundary Scan?

Boundary scan is a methodology allowing complete controllability and observability of the boundary pins of a JTAG compatible device via software control.

Boundary Scan Architecture



BOUNDARY SCAN PRINCIPLE

n How does it work?

The top level schematic of the test logic defined by IEEE Std 1149.1 includes three key blocks:

The TAP Controller

This responds to the control sequences supplied through the test access port (TAP) and generates the clock and control signals required for correct operation of the other circuit blocks.

The Instruction Register

This shift register-based circuit is serially loaded with the instruction that selects an operation to be performed.

The Data Registers

These are a bank of shift register based circuits. The stimuli required by an operation are serially loaded into the data registers selected by the current instruction. Following execution of the operation, results can be shifted out for examination.

JTAG Test Access Port

- n The JTAG Test Access Port (TAP) contains four pins that drive the circuit blocks and control the operations specified. The TAP facilitates the serial loading and unloading of instructions and data.

The four pins of the TAP are:

- n TMS – Test Mode Select
- n TCK – Test Clock
- n TDI - Test Data Input
- n TDO – Test Data Output

JTAG Test Access Port (Contd)

The function of each TAP pin is as follows:

- n TCK - this pin is the JTAG test clock. It sequences the TAP controller as well as all of the JTAG registers
- n TMS - this pin is the mode input signal to the TAP Controller. The state of TMS at the rising edge of TCK determines the sequence of states for the TAP controller.

JTAG Test Access Port (Contd)

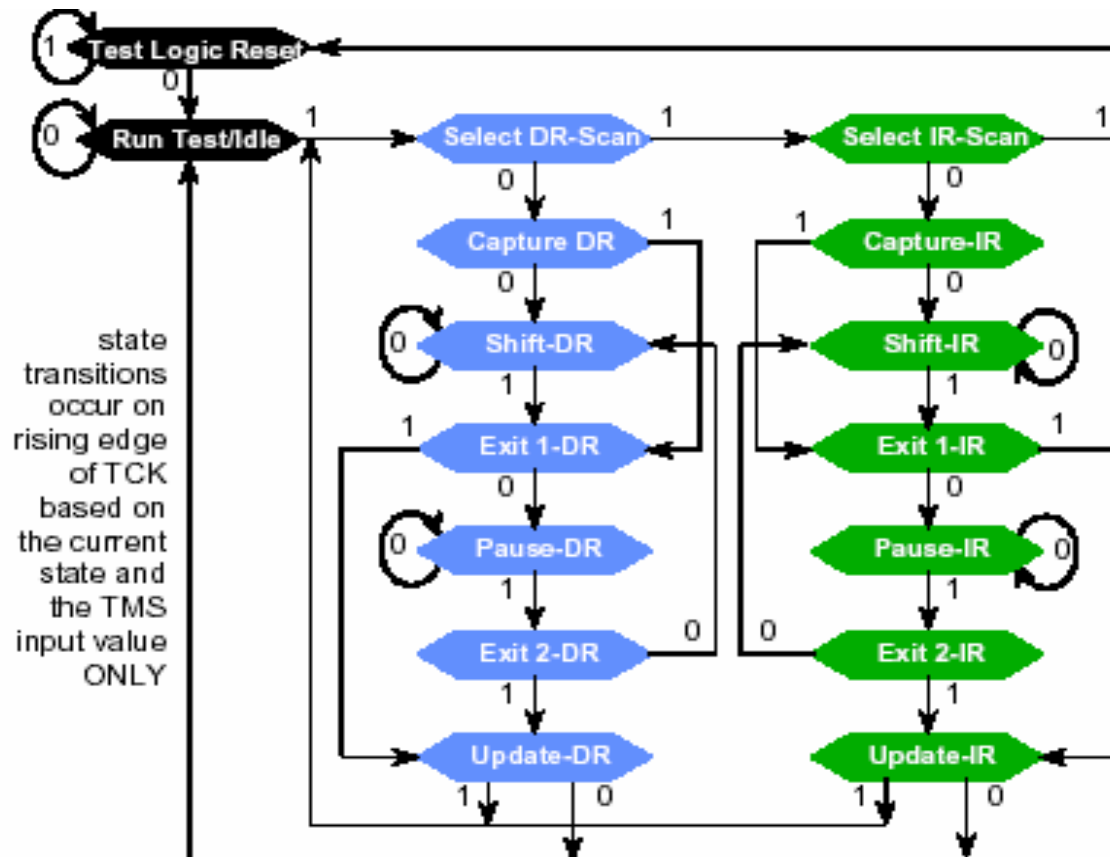
- n **TDI** - this pin is the serial data input to all JTAG instruction and data registers. TDI is sampled into the JTAG registers on the rising edge of TCK.
- n **TDO** - this pin is the serial data output for all JTAG instruction and data registers.. TDO changes state on the falling edge of TCK and is only active during the shifting of data through the device. This pin is three-stated at all other times

JTAG TAP Controller

The JTAG TAP Controller is a

1. 16-state finite state machine, that controls the scanning of data into the various registers of the JTAG architecture.
2. The state of the TMS pin at the rising edge of TCK is responsible for determining the sequence of state transitions.
3. There are two state transition paths for scanning the signal at TDI in to the device,
 - i one for shifting in an instruction to the instruction register ,and ,
 - i one for shifting data into the active data register as determined by the current instruction.

JTAG TAP Controller logic



■ 16-state TAP provides 4 major operations:

- RESET
- RUN-TEST
- SCAN-DR
- SCAN-IR

■ Scans consist of 3 primary steps:

- CAPTURE
- SHIFT
- UPDATE



Data Registers

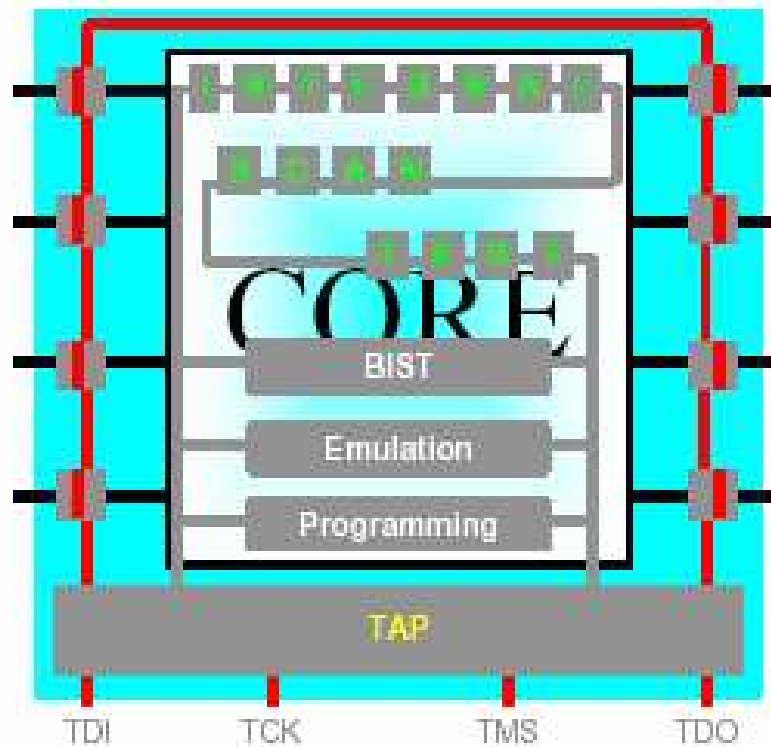
- n The *Device ID* register (*IDR*) reads-out an identification number which is hardwired into the chip.
- n The *Bypass* register (*BR*) is a 1-cell pass-through register which connects the TDI to the TDO with a 1-clock delay to give test equipment easy access to another device in the test chain on the same board.
- n The *Boundary Scan* register (*BSR*), intercepts all the signals between the core-logic and the pins.

Test Process

The standard test process for verifying a device or circuit board using boundary-scan technology is as follows:

- n The tester applies test or diagnostic data on the input pins of the device.
- n The boundary-scan cells capture the data in the boundary scan registers monitoring the input pins.
- n Data is scanned out of the device via the TDO pin, for verification.
- n Data can then be scanned into the device via the TDI pin.
- n The tester can then verify data on the output pins of the device.

REAL JTAG APPLICATIONS



- Scan access to chips, boards, systems for:
 - Design verification/debug
 - Manufacturing test
 - Hardware/software integration
 - Field test/diagnostics
- Access built-in self-test (BIST)
- Access on-chip/in-circuit emulation (ONCE/ICE)
- Access in-system programming (ISP) of PLDs/EEPROMs
- Let your imagination run wild!!!

References

- n http://www.ee.ic.ac.uk/pcheung/teaching/ee3_DSD/ti_jtag_seminar.pdf
- n <http://www.inaccessnetworks.com/projects/ianjtag/jtag-intro/jtag-intro.html>
- n http://toolbox.xilinx.com/docsan/3_1i/data/common/jtg/dppa/appa.htm