UNCC, Department of Electrical and Computer Engineering

ECGR 6185, Spring 2006, Lab #1, Due: 2/27/06, at the end of class (20 points)

Lab Partners: _____ and _____

Prelab:

1. Write the truth table for the exclusive or (1 point)

2. Write the circuit for the exclusive-or using two inverters, two and gates, and one or gate. (1 point)

In-class lab (2/27/06):

Follow the lab exercise described in the document "Xillinx ISE 7.1i Schematic Design Entry Reference Guide." You will use schematic capture to design the exclusive-or circuit, synthesize the circuit, and download the functionality to the FPGA board. Once you have completed the exercise, show the TA your work, then return the board. (6 points each)

Show the TA your schematic. _____

Show the TA your working FPGA board showing the working exclusive-or circuit _____

Turn your board back in _____