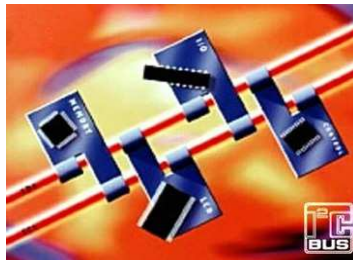


**ECGR-6185
Advanced Embedded Systems**

I2C(Inter-IC Bus)

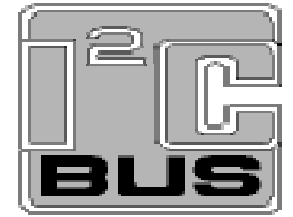


Venkat Dronamraju



UNC CHARLOTTE

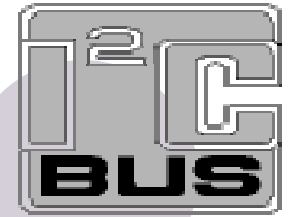
University of North Carolina- Charlotte



Topics Discussed

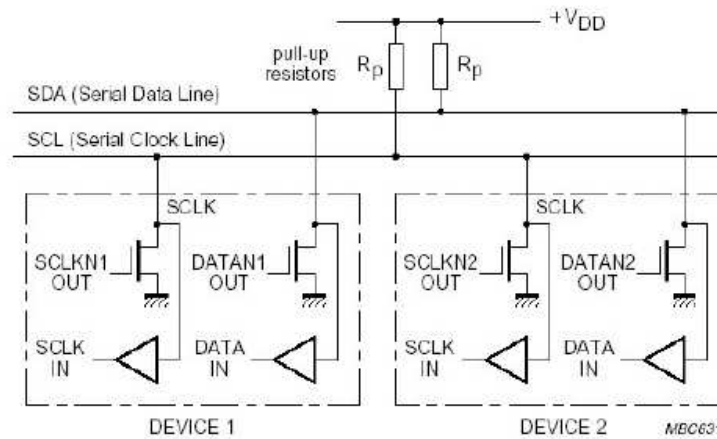
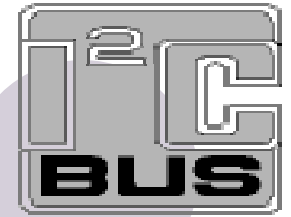
- 1 Introduction to I2C
- 1 Hardware
- 1 Addressing mode and Transfer rate
- 1 Protocol Mechanism (Including read/write/Ack process)
- 1 Modes and Versions
- 1 Advantageous and limitations
- 1 Embedded Systems Perspective

Introduction to I2C



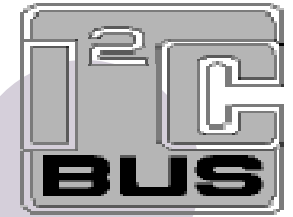
- 1 It is a low bandwidth, short distance bus protocol developed by Philips in early 1980's.
- 1 It provides a simple way to talk between IC's by using 2 wires SCL (Serial Clock) and SDA (Serial Data). Both the lines are bi-directional.
- 1 I2C protocol provides
 - Device addressing
 - A read/write flag
 - Simple Ack mechanism
 - Broadcast (Special Feature)
 - 10-bit extended addressing
 - Device count limit : Max capacitance 400pF
 - Three versions 1.0(1992) 2.0(1998) 2.1(2000)

I2C Hardware

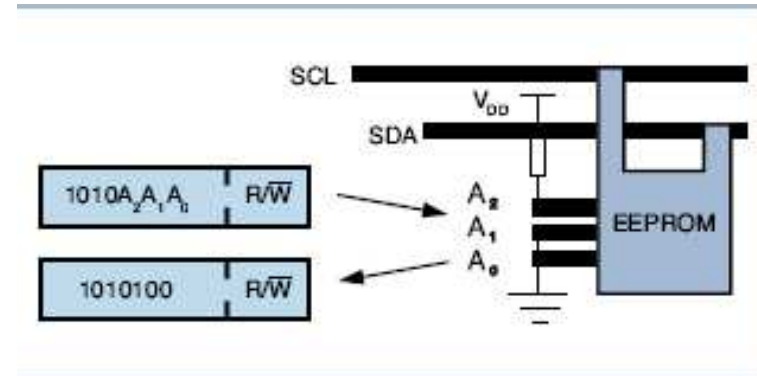


- 1 SCL and SDA are pulled up via pull-up resistors to V_{DD} voltage. Hence when bus is idle it will always be in high state.
- 1 Bus structure is a wired AND. When one device pulls a line low it stays low.

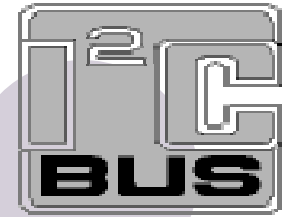
Addressing modes



- 1 Built-in addressing scheme hence eliminating needs for address decoding hardware.
- 1 Total 120 devices can be addressed. Additional 8 address are used for special purposes.
- 1 Every device hooked up to the bus has its own unique address.
- 1 MSB is transmitted first.
- 1 MSB is fixed for all devices. For Ex 1010à EPROM.

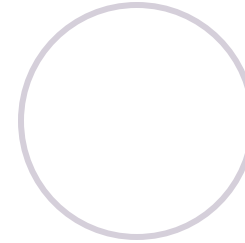
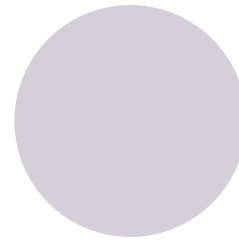


10 bit addressing mode



- 1 The 2 address bytes are transmitted.
- 1 1st byte of the format [11110xx (R/W)]. The 2 addressable bytes are the MSB of 10 bit address.
- 1 2nd byte [Fixed MSB xxx (R/W)]

Transfer rate



- 1 I2C offers three levels of data speed

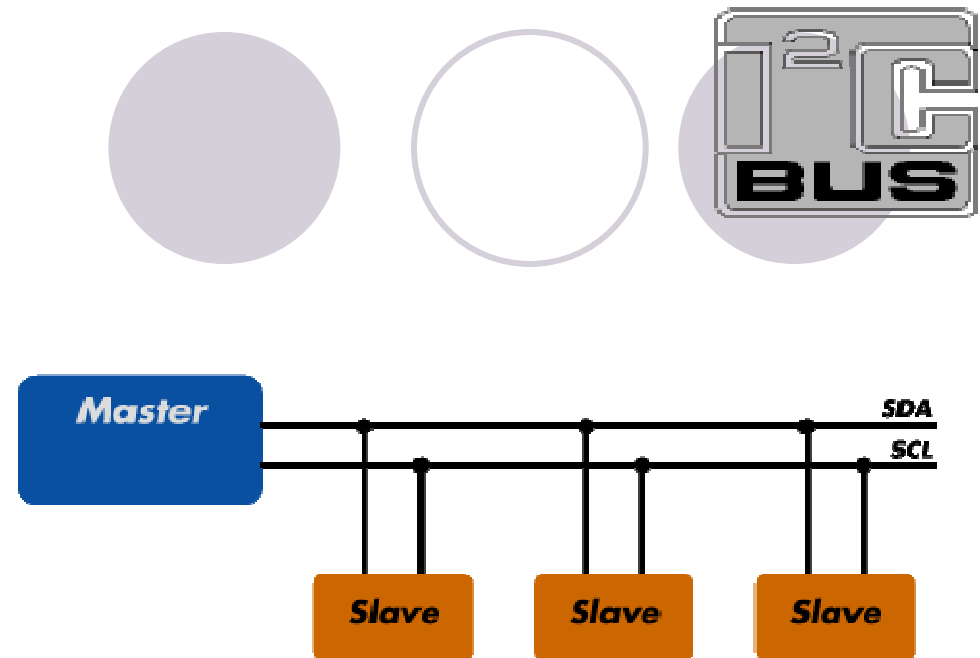
Standard Mode 100Kbps

Fast Mode 400 kbps

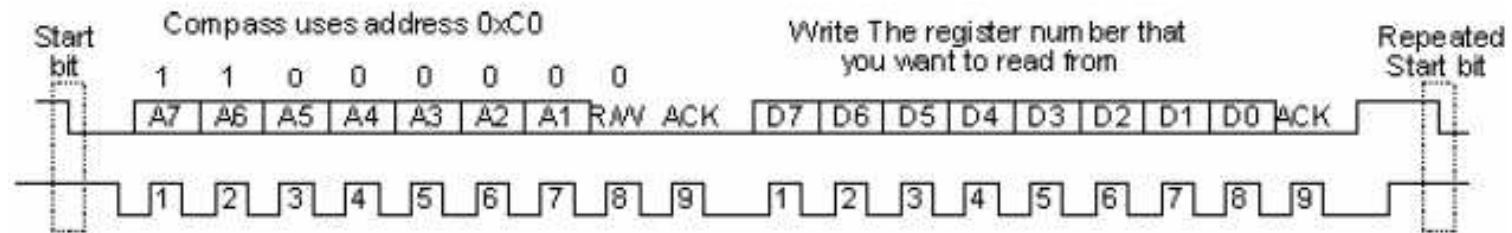
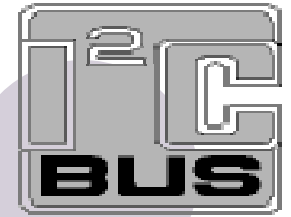
High-Speed Mode 3.4 Mbps

Protocol mechanism

- 1 I2C implements master-slave configuration.
- 1 Master initiates communication and controls the clock signal.
- 1 Slaves are responsible for monitoring the bus and responds only to it own address.
- 1 In a system there can be 2 masters. Both will have equal priority.

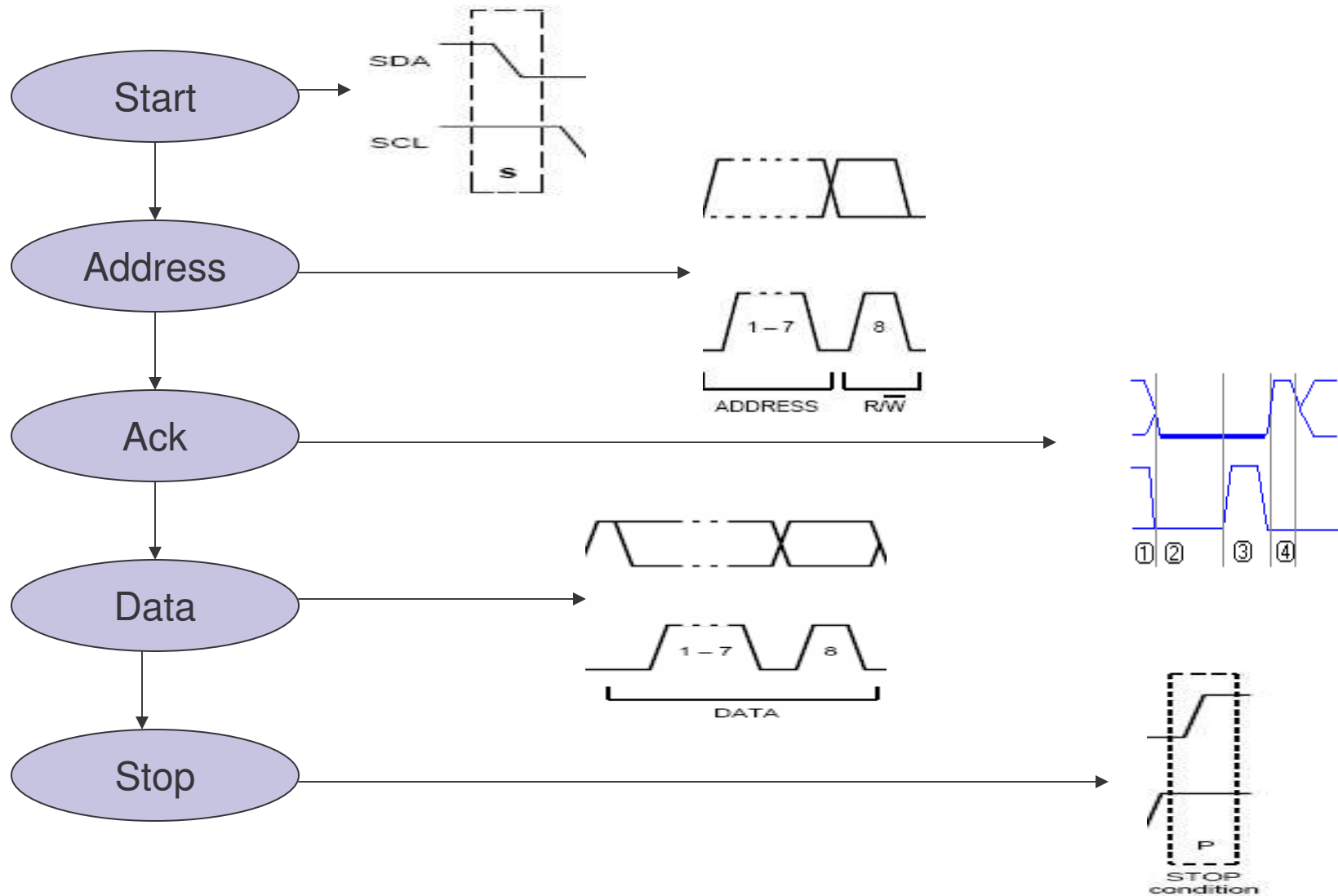
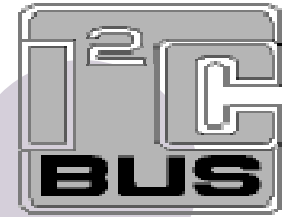


Protocol Mechanism

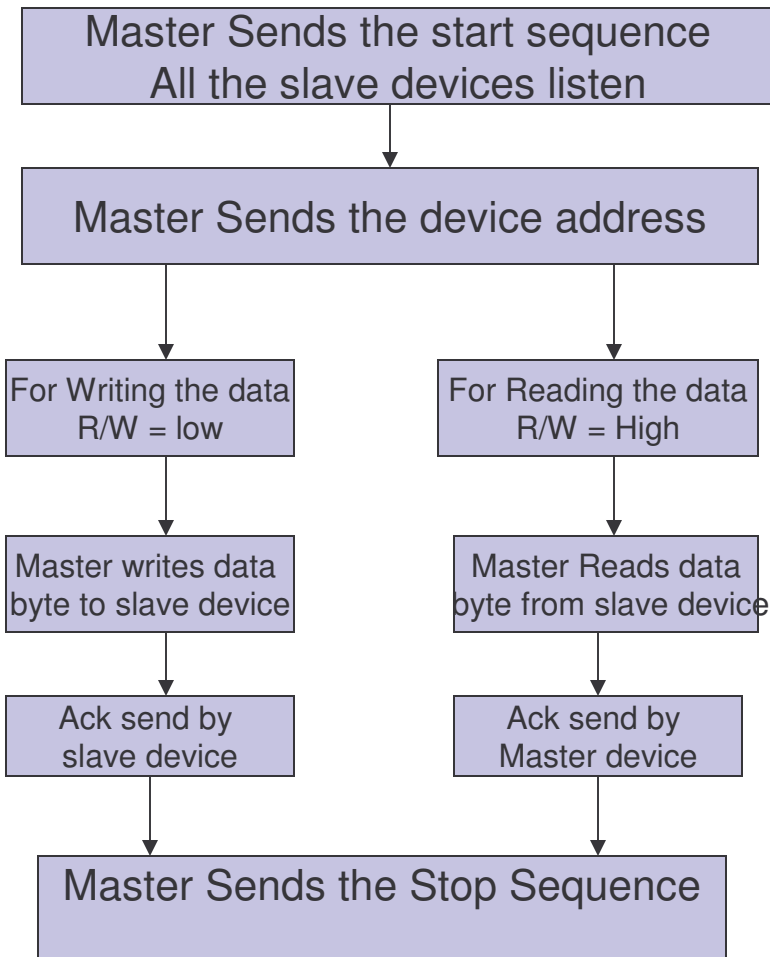
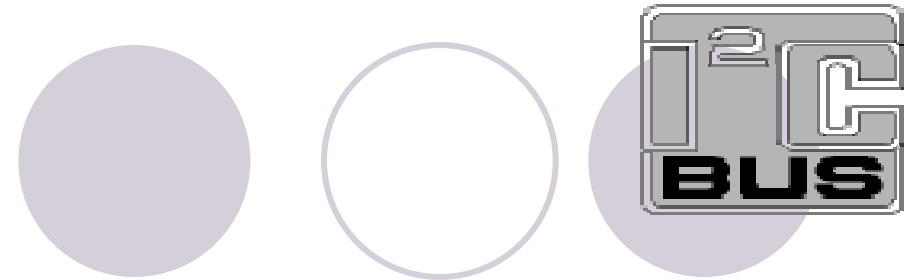


- [Master sends START sequence.
- [Followed by 7 address bits with MSB first.
- [8th bit determines R/W
- [Followed by 8 bit data transmitted via SDA while SCL will have clock pulses.
- [Slave ACKnowledges every 8 bit of data received.
- [After the data transfer. Master sends stop sequence.

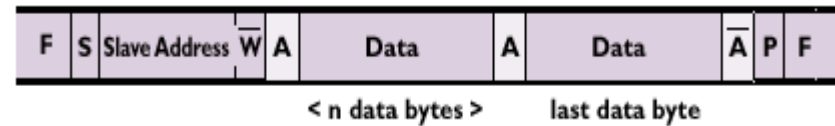
Protocol Mechanism (contd.)



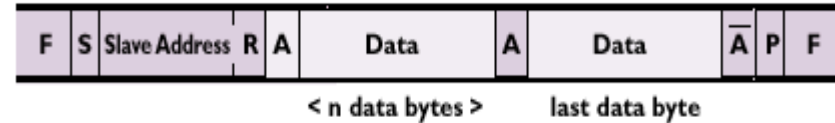
Read/ Write process



Write Data

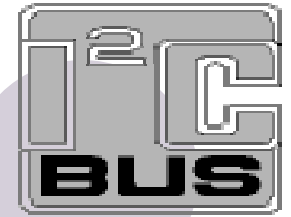


Read Data



- S = Start condition A = Acknowledge
- F = Free $\overline{R/W}$ = read / Not write
- P = Stop condition \overline{A} = Not Acknowledge

Special Address and Extensions



| Address | R/W | Designations |
|----------------------|-----|--|
| 0000-000 | 0 | General Call address |
| 0000-011 | 0 | Reset and write the programmable part of slave address |
| 0000-010 | 0 | Without Reset the device address can be changed |
| 0000-011 to 1111-1xx | x | For future purpose |
| 1111-0xx | x | 10 bit addressing |

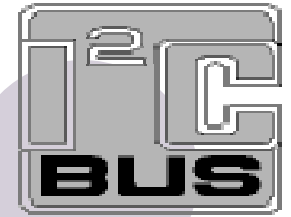
Versions

| | V1.0(1992) | V2.0(1998) | V2.1(2000) |
|----------|--|--|--|
| Omitted | <ol style="list-style-type: none">1.No software programming of slave device2. Low speed mode | <ol style="list-style-type: none">1.0.6 V at 6mA requirements for the output stages2. Fast mode | <ol style="list-style-type: none">1.Timing parameters in Hs mode have been relaxed |
| Added | <ol style="list-style-type: none">1.Fast mode added2.10 bit addressing added3. Slope control and input filtering added | <ol style="list-style-type: none">1.Hs mode(3.4Mbit/s)2. Bi-directional level shifter | <ol style="list-style-type: none">1. Stretching of clock signal possible |
| Replaced | | Fixed Input levels are replaced by bus voltage-related levels | |

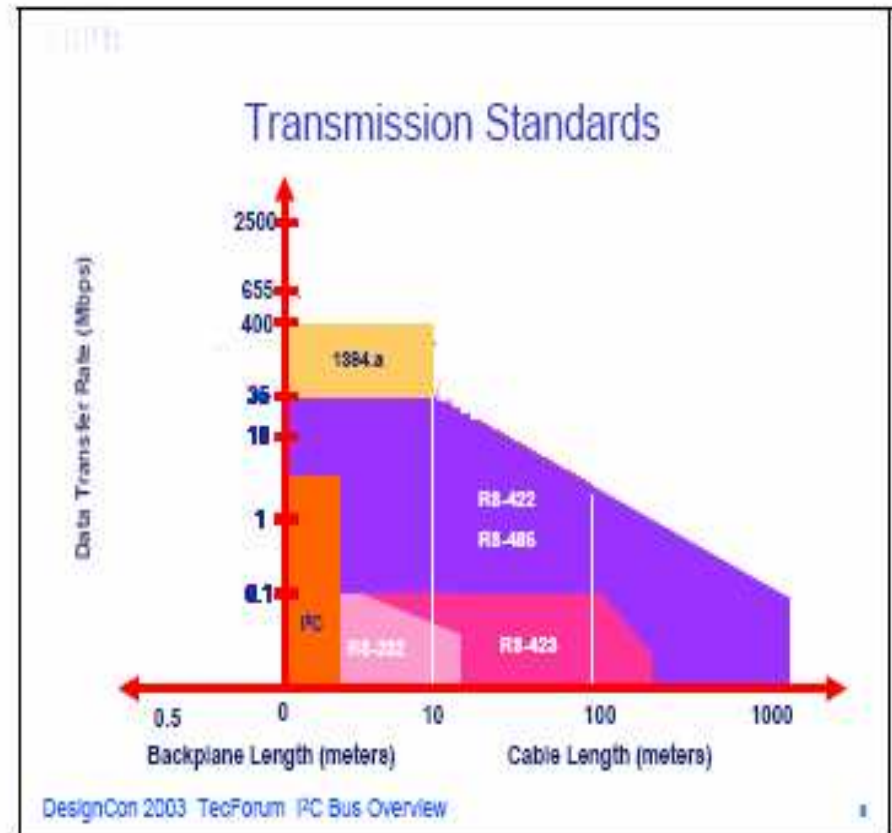
Modes

| Modes | Speed | Physical parameters | Noise level | Pull-up resistors |
|----------|---|---|---|--|
| Standard | 100Kbit/s | Bus level capacitive load | -- | Passive |
| Fast | 400Kbit/s | Physical parameters same as Standard mode | Schmitt Triggers to suppress noise | 1.Pull resistors below 200pF 2.Between 200 to 400pF active Pull-ups |
| Hs | 3.4Mbit/s (Downward Compatible) High speed clock and data (SCLH and SDAH) | 1.Same as Fast mode 2.Arbitration and clock sync not performed | 1.Spike suppression and Schmitt trigger. 2. Signals called SCLH and SDAH | For SCLH there is combination of open drain pull-down and current source pull-up |

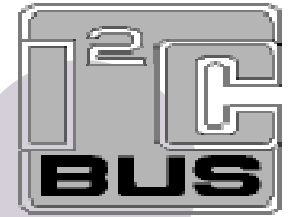
Comparison of other Communications



| Standard | Speed |
|---|------------------------|
| I2C(industrial & SM bus), Fast mode I2c | 100KHz, 3.4 MHz |
| SPI | 100kHz(Original speed) |
| CAN (High Speed) | 1MHz |
| USB(1.1) | 1.5MHz or 12MHz |
| SCSI (Parallel port), Fast SCSI | 40 MHz, 8-80MHz |
| Firewire | 400MHz |
| USB(2.0) | 480MHz |



Advantages and Limitations



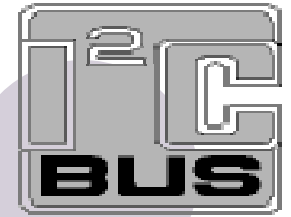
Advantages

1. 2 wire communication.
2. ICs can be added or removed from system with out effecting any other circuit on the bus.
3. Integrated addressing and data transfer protocol allow system to be completely software dependent.
4. Don't require device drivers(plug and play).
5. Low power consumption
6. Cost Effective.

Limitations

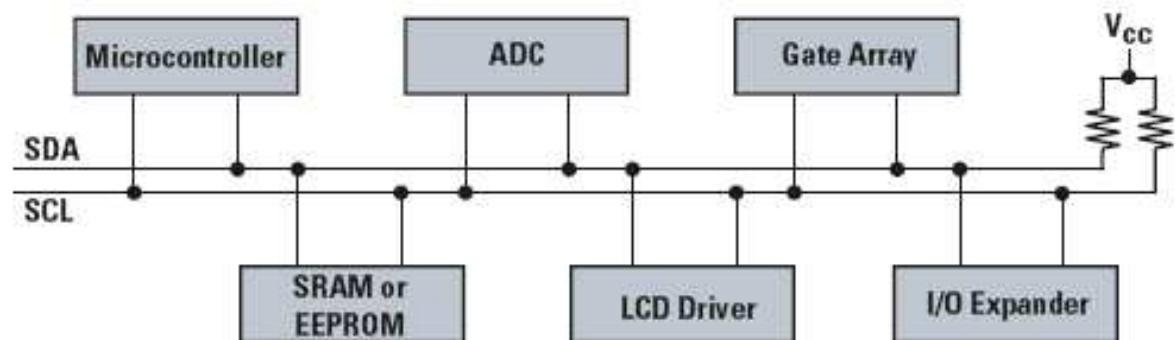
1. Get reflections at especially at high speeds. (To avoid this use dynamic resistor or current source)
2. Ghost signals may disturb transmission and corrupt the data.
3. Long lines present capacitive load.
4. No time outs in standard mode.

Embedded systems perspective



1. Popular in low end spectrum of communication, especially “inside the box communication.”[7]
2. Extremely modest in its hardware resources needs.
3. Low band-width, provides good support for various slow on-board peripheral devices.[7]
4. Used widely in consumer electronics and multimedia applications, where typical application include RF tuner, video decoder and encoders and audio processors.
5. Cost and complexity don't scale up with no of devices on the bus.[7]

6. Typical Example:



References

[1]. Dr James Conrad
<http://www.coe.uncc.edu/~jmconrad>
Accessed : March 2006

[2]. Philips Semiconductors
<http://www.semiconductors.philips.com>
Accessed : March 2006

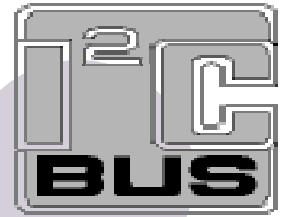
[3]. Philips Semiconductors
http://www.semiconductors.philips.com/acrobat_download/literature/9398/39340011.pdf
Accessed : March 2006

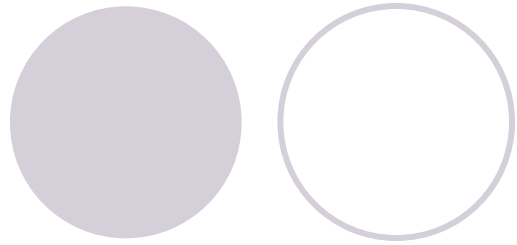
[4]. <http://www.esacademy.com/faq/i2c/index.htm>
Accessed : March 2006

[5]. <http://www.totalphase.com/support/i2c/>
Accessed : March 2006

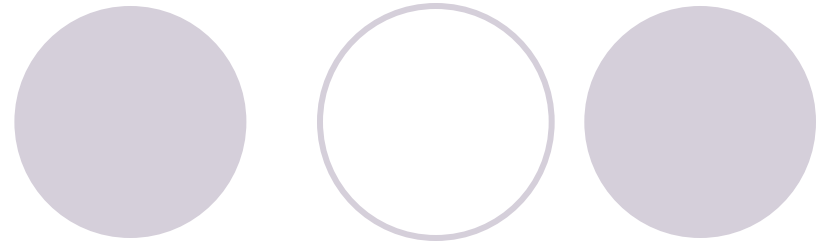
[6]. <http://www.i2c-bus.org/highspeed/>
Accessed : March 2006

[7] <http://www.embedded.com/story/OEG20010718S0073>
Accessed : March 2006





Thank you !



Questions?

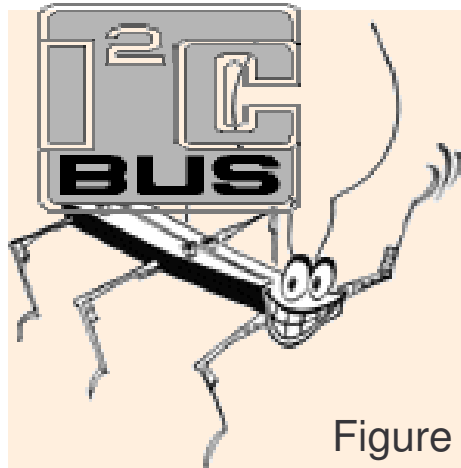


Figure [1]

