High Performance Space Computing

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Outline

Challenges

As more complex and expensive machines are sent to the space, there are challenges:

- Computers are not fast enough
- More power are consumed as the complexity increases
- Raw data is too large to transmit between computers and ground base system
- Hardware reliability
- Fixed hardware architecture

Solutions

- Multi-core, multiprocessor, parallel computing
- On-chip data processing
- Multi-core voting system
- Programmable hardware

Block Diagram

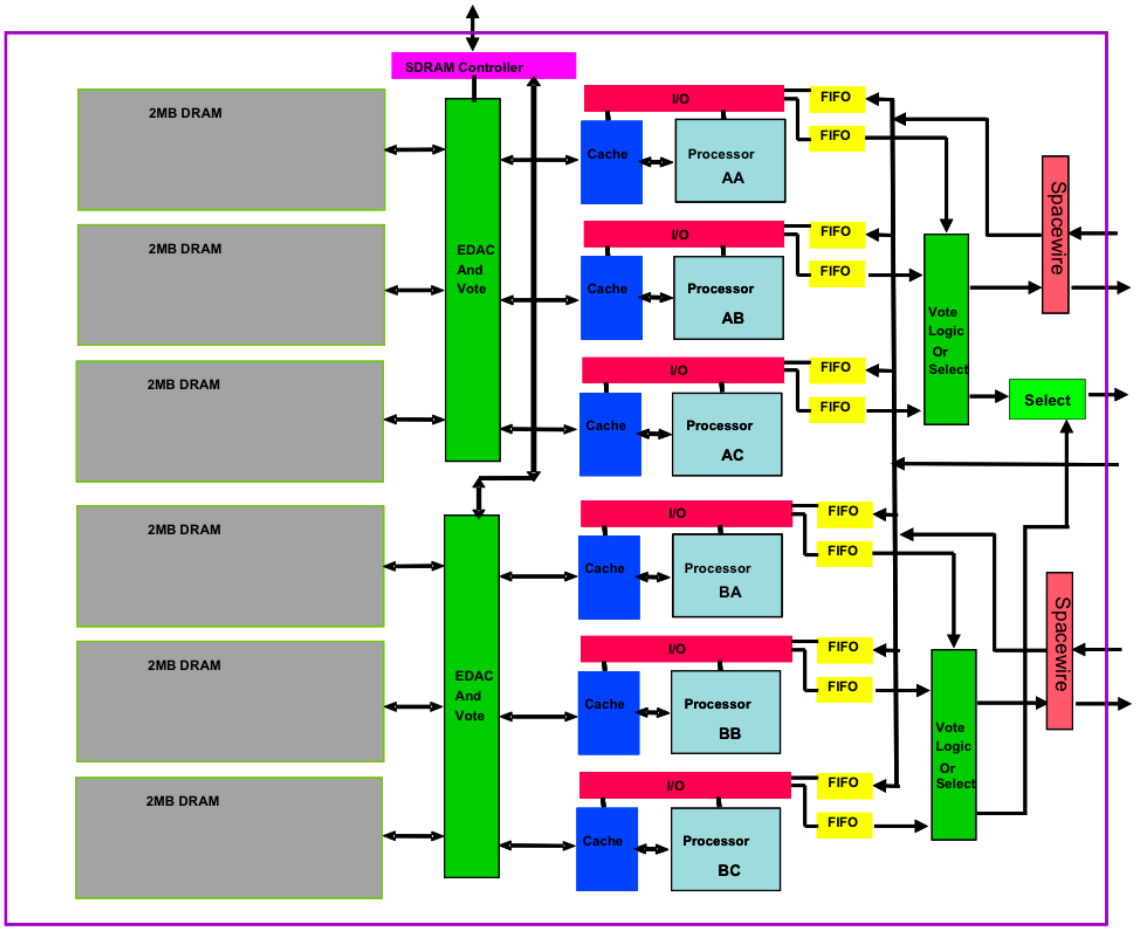

Figure 1: FPASP7.0 Block Diagram

Processor Core

- Floating Point Application Specific Processor (FPASP)
- 3 pipeline stages for floating point operations
- 2 floating point multiplies, add/sub per clock cycle on one core
- 100% synthesizable VHDL

Embedded Dynamic Random Access Memory (EDRAM)

- Reduced leakage current relative to SRAM
- 592 bits wide (512 data bits, 64 error correction bits)
- Bits error will cause maskable interrupt to processor

Inputs and Outputs

- Each processor has 8 Kbyte input and 8 Kbyte output FIFO
- Ethernet I/O, 10 Gbit/second
- Spacewire: low voltage differential signaling pairs, up to 625 Mbits per second

Evaluation board

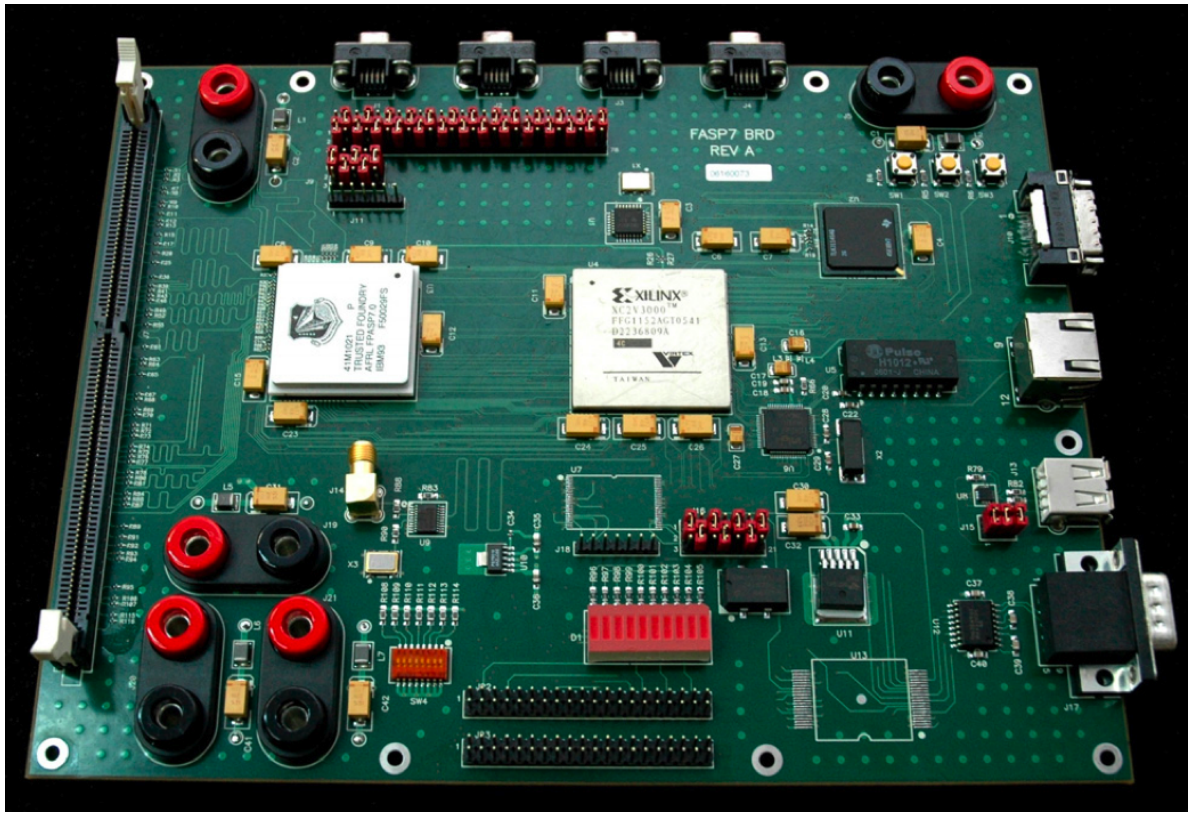

Figure 2: Evaluation board with 10/100 Ethernet, 10 Gbit Ethernet, Spacewire, USB, RS-232 and header pins

Board Test

- Regression tests
- Tests for Operating System, Real-Time Executive for Multi-Processor Systems
- Power consumption: 1 watt for 6 processor cores, caches, and EDRAMS
- Radix-4 4096 point FFT: 63% utilization rate
- 8 complex coefficients 4096 point FIR filter: 96% utilization rate

Multi-Processor MTI Example (Conceptual)

- Real-time radar signal
- Input data: 16 channels, real time flow of 866 Mbytes/sec
- Approach: PRI-staggered post doppler approach to space-time adaptive processing (STAP)
  - Pulse compress in range, 314 MFLOPs
  - Doppler process, 180 MFLOPs
  - Calculate beamforming weights with PRI-staggered STAP, 156 MFLOPs
  - Form multiple adaptive receive beams and make detections, 232 MFLOPs

Conclusion

- A power efficient, scalable high performance computing architecture
- Embedded DRAM with triple voting processors
- Suitable for high data rata floating point intensive processing