An Embedded System with uClinux based on FPGA

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Abstract

Nowadays Field Programmable Gate Arrays (FPGAs) have become so affordable that they can be used to replace ASICs in some fields such as embedded systems in consumer electronic industry. In the paper, we design an embedded system with uClinux OS (operating system) based on FPGA. The way and experiences of the co-design of HW/SW are presented. The paper also gives an application of MPEG2-player on the embedded system and the comparison with other embedded system based ASICs.

1. Introduction

Embedded systems, which are widely used in consumer electronic appliances, are characterized by a rapidly increasing complexity and shorter product cycles. The designers are under more and more pressure to reduce design cycles usually in the presence of continuously changing specifications. This explosive growth in the embedded systems market has been fueled by rapid prototyping technologies. The ability to quickly program microprocessor memories in-circuit and reconfigure field-programmable digital hardware is critical to embedded systems engineers who must meet ever shortening development cycles [1].

FPGAs have become more and more popular for implementation of logic circuits. The flexibility of FPGAs has made them suitable for implementation of embedded SOPC systems, where a complete system fits on a single programmable chip. A processor unit in such a system is usually a soft-core processor. A soft-core processor is a microprocessor fully described in software, usually in an HDL, which can be synthesized in programmable hardware, such as FPGAs. Soft-core processors implemented in FPGAs can be easily customized to the needs of a specific target application. The two major FPGA manufacturers provide commercial soft-core processors. Xilinx offers its MicroBlaze processor [2], while Altera Nios II processors [3]. In this paper, we design the embedded system based on the Nios II soft-core processors.

This paper is organized into 4 sections. In section 1, a brief description of embedded system based on FPGAs is introduced. The hardware architecture, the selecting of hardware platform and the design of hardware of embedded system on FPGAs are presented in detail in section 2. In section 3, uClinux OS and the porting of it are introduced, then the paper gives some important user applications under uClinux for consumer electronic, furthermore the design of mpeg2-player by co-design of hardware and software is brought up, which use libmpeg2[4] and libsdl[5]. In the final section, this paper focuses on the comparison between the embedded systems based on ASICs and FPGAs and analyzes the important characteristics of them.

2. Hardware system

2.1. Hardware architecture of system

In the paper, we use SOPC builder provided by Altera to design the hardware system, which provides designer Nios II soft-core processor and some peripherals and allows designer to customize peripherals. This makes designer have more freedom to extend the peripherals of the embedded systems, however the designer must give HDL design of interface between the avalon bus and peripherals.

Fig.1 gives our design of hardware of embedded system. In our design, we designed the Ethernet controller, SD card controller, Audio controller, LCD controller, USB controller to extend peripherals, which can make our embedded system have more functions and more available to be supported by operating system.

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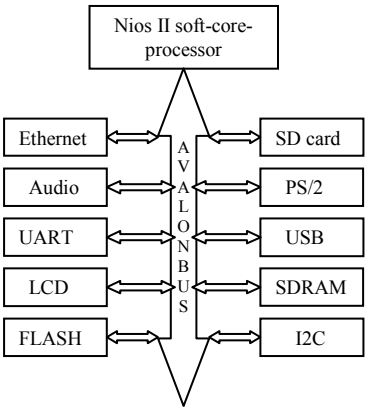

Fig.1 Block diagram of hardware architecture

2.2. Hardware platform

Our design system is based on Altera DE2-70 development board and TRDB_LCM LCD. The core of the board is Cyclone II EP2C70 FPGA, which has 68416 LEs (logic elements) and 250 M4K RAM blocks (1152000bits). The DE2-70 board includes peripheral interfaces, by integrating control chips as follows:

- ◆ Flash (with 8M S29GL064)
- ◆ SDRAM (with 32M IS42S16160B)
- ◆ Ethernet (with DMA9000A)
- ◆ USB host / client (with ISP1362)
- ◆ Audio (with WM8731)
- ◆ VGA (with ADV7123)
- ◆ SD card socket
- ◆ RS232
- ◆ IrDA
- ◆ PS/2

The photo of DE2-70 board and TRDB_LCM LCD is shown in Fig. 2.

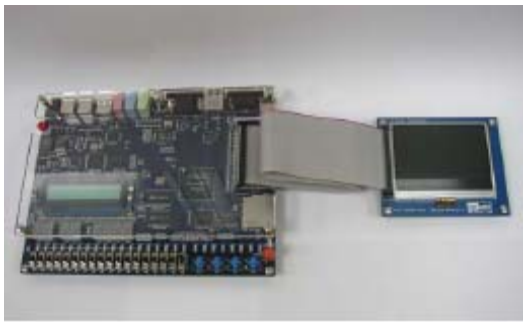
Fig.2 Hardware platform of embedded system

2.3. Hardware design

In the paper, we design the hardware by the quartus II and SOPC builder. The clock rate of the soft-core-processor based on CYCLONE II EP2C70 is up to 112MHZ, so the performance of soft-core-processor can be up to 112DMIPS(Million Instructions Per Second). A part of design of hardware in SOPC builder is shown in Fig.3.

⊞ **cpu**	Nios II Processor	**sys_clk**	**0x00800800**
⊞ **flash_tristate_bridge**	Avalon-MM Tristate Bridge	**sys_clk**	
⊞ **ext_flash**	Flash Memory (CFI)	**sys_clk**	0x00000000
⊞ **sdram**	SDRAM Controller	**sys_clk**	0x02000000
⊞ **sys_clk_timer**	Interval Timer	**sys_clk**	**0x00801800**
⊞ **ISP1362**	ISP1362_IF	***multiple***	*multipla*
⊞ **lcd_i2c_scl**	PIO (Parallel I/O)	**sys_clk**	**0x008018a0**
⊞ **lcd_i2c_en**	PIO (Parallel I/O)	**sys_clk**	**0x00801900**
⊞ **lcd_i2c_sdat**	PIO (Parallel I/O)	**sys_clk**	**0x00801920**
⊞ **ps2_0**	PS2 Serial Port	**sys_clk**	**0x00800010**
⊞ **dm9000**	DM9000A_IF	**sys_clk**	**0x00000000**
⊞ **uart**	UART (RS-232 Serial Port)	**sys_clk**	**0x00801880**
⊞ **lcd_sgdma**	Scatter-Gather DMA Controller	**sys_clk**	**0x00801400**
⊞ **lcd_ta_sgdma_to_fifo**	Avalon-ST Timing Adapter	**sys_clk**	
⊞ **lcd_pixel_fifo**	On-Chip FIFO Memory	***multiple***	
⊞ **lcd_ta_fifo_to_dfa**	Avalon-ST Timing Adapter	**sys_clk**	
⊞ **lcd_64_to_32_bits_dfa**	Avalon-ST Data Format Adapter	**sys_clk**	
⊞ **lcd_pixel_converter**	Pixel Converter (BGR0 --> BGR)	**sys_clk**	

Fig.3 Design of hardware of FPGA

3. Software system design

3.1. Embedded operating system

FPGA processor cores are now supported by a number of embedded operating systems. By incorporating an operating system into our design, we can easily enhance the performance of the embedded system and extend a lot of functions and easily use an efficient approach to mange all the peripherals of the embedded system.

In our design, we incorporate uClinux into our embedded system, which does not require a memory management unit (MMU). It has such features as open source, stability, powerful network function and excellent file system [6]. The newest edition of uClinux for Nios II is included in nios2-linux-20080619.tar [7] which uses Linux kernel 2.6.26 and can be downloaded from the website (ftp://ftp.altera.com/outgoing/nios2-linux-20080619.tar).

uClinux is a derivative of Linux, which is designed specially for microprocessor without memory management unit(MMU). Accomplishment of the porting of uClinux includes boot loader, uClinux kernel, file system. Fig.3 gives the block diagram of uClinux.

With porting uClinux for our hardware system, we can use all the device under operating system such as LCD for framebuffer, SD card for root device, PS/2 for keyboard and USB for mouse or removable mass device, except audio device, because which not only requires the device driver for WM8731 but also the platform driver for the audio device, such as PCM or AC97 for Nios II platform which are not included in uClinux for Nios II.

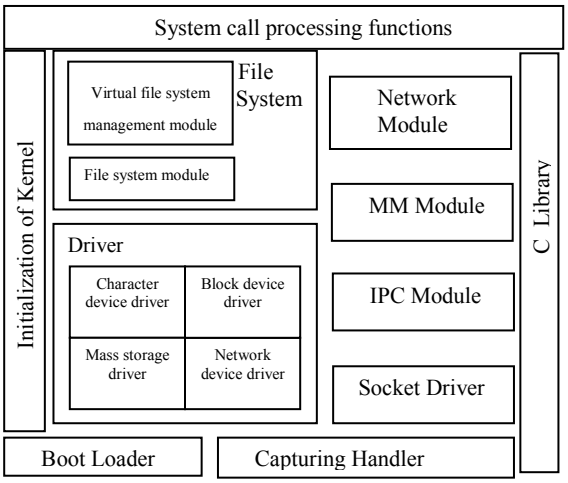

Fig.4 Architecture of uClinux

3.2. User application

In our design, we also incorporate a lot of user application and lib, some important application and as follows:

(1) Nano-X which is an open-source GUI (Graphical User Interface) for embedded system [8] [9];

(2) SDL (Simple DirectMedia Layer) which is a cross-platform multimedia library designed to provide low level access to audio, keyboard, mouse, joystick, 3D hardware via OpenGL, and 2D video framebuffer [5].

(3) Links which is a fast, lightweight text and graphical web-browser with support for HTML tables and frames [10].

(4) BusyBox which combines tiny versions of many common UNIX utilities into a single small executable [11].

3.3. Accomplishment of MPEG2-player

Our MPEG2 player is designed based on libmpeg2 (a free MPEG-2 video stream decoder). The playing of MPEG-2 video stream decoder needs the framebuffer device and audio device, however the audio device in DE2-70 is not directly used under the operating system because that there is no driver for audio device (WM8731) under Nios II platform.

3.3.1. Control of audio device

In our design, we creatively use the audio device by IO programming in user space of uClinux instead of writing device driver which will cost the designers a lot of time to finish.

We can use the port address of the devices defined in SOPC builder for IO programming to control the device, which is the flexibility of soft-core processor of FPGAs, so after the initiation of audio device, we can directly write data to the audio device and read data from it. In the mpeg2-player program, we only write data to the audio device, what we have to do are listed as follows:

(1) Initiate the audio device according to the datasheet of WM8731 by controlling I^2C, Fig.5 lists AUDIO_Init function which is designed to initiate audio device, I^2CWrite is a function which control I^2C hardware for audio device.

(2) Set the sample rate and channel of audio device

(3)Writing data to audio device and control FIFO of audio component designed in SOPC builder

```
int AUDIO_Init(void){
   int complete = 1;
    printf(("AUDIO_Init...\r\n"));
    if(complete)
       complete = I²CWrite(15, 0x0000);
    if(complete)
       complete = I²CWrite(9, 0x0000);
    if(complete)
       complete = I²CWrite(0, 0x0017);
    if(complete)
       complete = I²CWrite(1, 0x0017);
    if(complete)
       complete = I²CWrite(2, 0x005B);
    if(complete)
       complete = I²CWrite(3, 0x005B);
    if (complete)
       complete = I²CWrite(4, 0x0015 | 0x20 | 0x08 | 0x01);
    if (complete)
       complete = I²CWrite(5, 0x0000);
    if (complete)
       complete = I²CWrite(6, 0);
    if (complete)
       complete = I²CWrite(7, 0x0042);
    if (Complete)
       Complete = I²CWrite(8, 0x0002);
    if (Complete)
       Complete = I²CWrite(9, 0x0001);
    printf("audio_Init %s\r\n",complete?"sucess":"fail");
    return complete;
```
Fig.5 AUDIO_Init function

3.3.2. MPEG2-player design

We choose SDL for video output of MPEG2-player on Nano-X, so we must cross-compile SDL and libmpeg2 which must be configured with the flag that enable SDL for video output.

Fig.6 shows the design of flowchart of mpeg2-player. The program uses the mpeg2_open function to open mpeg2 files. Before setting sample rate and channels of audio device, we must use mpeg2_has_audio function to get the sample rate, channels and total audio samples and use mpeg2_has_video function to get frame rate, width, height and total video frames from mpeg2 file. Moreover, audio output and video output are executed by two threads so they can be synchronous. Audio output can be completed by writing decoded audio data to the base address of left and right channels. Video output can be implemented by calling the SDL function to output decoded video data on the LCD.

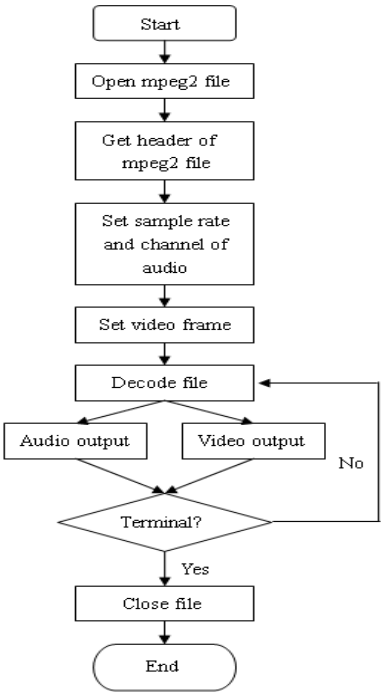

Fig.6 flowchart of mpeg2-player

4. Performance Comparison

Comparing with other embedded systems without MMU based on ASICs, the embedded system based on FPGAs offer the same functions by porting uClinux system except the performance of processor. Because of slower clock rate, soft-core processor offers a lower performance and consumes more power than ASICs. However, the soft-core processor has more flexibility. The soft-core processor is a reconfigurable IP core, which can reduce the design cycle which can be a key factor for consumer electronic industry. The peripherals can be easily added to the hardware system with less confinement according to the requirements of customers. The embedded system can be added more specialized functions executed by LEs. Furthermore, the designer can build multi-processor in one FPGA, which will enhance the performance of embedded system.

5. Conclusions

In this paper, a whole embedded system based on Nios II soft-core processor is designed including some important user application of operating system. This can be a novel design of embedded system for consumer electronic industry. From the discussion above, although the performance of soft-core processor is lower than ASICs, the designer can let existing external programmable logic elements to execute the CPU-consuming program such as video decode and audio decode, which can compensate the lower performance of it. Although the soft-core processor based on FPGAs can be promising, there is a lot of effort should be done such as increasing the clock rate and decreasing power consuming.

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