$n \times 2^{-127}$ with BIAS

Exponent BIAS

$-127 + 127 = 0$

$m \times 2^{128}$

BIAS

$128 + 127 = 255$

Practice

$17.625_{10} \longrightarrow$

single precision floating point

17 .5 .125 ($\frac{1}{2} + \frac{1}{8}$)

10001.101 $\longrightarrow$

1.0001101×2^4

exponent $127+4 = 10000011$

significand $= 00011010000\ldots$

sign $= 0$

ECGR6185/8185 Quiz 17 - April 27, 2011

Your FULL name: Solution

1. Consider you are creating an embedded board with the following requirements:
   a. 512KB Flash ROM minimum
   b. 64 KB RAM minimum
   c. 100 external IO pins minimum
   d. 14 x 14 mm space maximum

Select the part that satisfies these requirements at the lowest cost. Justify your answer.

R5F56218BDLE#U0

Part No.	Program Memory (KB)	RAM (KB)	*Price (US$)	
R5F56216BDBG#U0	256	64	$5.84	
R5F56216BDFB#V0	256	64	$5.48	← Too large (20×20)
R5F56216BDFP#V0	256	64	$5.13	
R5F56216BDLE#U0	256	64	$5.48	
R5F56217BDBG#U0	384	64	$6.90	
R5F56217BDFB#V0	384	64	$6.55	← Too large
R5F56217BDFP#V0	384	64	$6.19	
R5F56217BDLE#U0	384	64	$6.55	
R5F56218BDBG#U0	512	96	$7.38	
R5F56218BDFB#V0	512	96	$7.03	← Too large
R5F56218BDFP#V0	512	96	$6.66	← Not enough I/O
R5F56218BDLE#U0	512	96	$7.03	
R5F562N7ADBG#U0	384	64	$7.14	
R5F562N7ADFB#V0	384	64	$6.79	← too large
R5F562N7ADFP#V0	384	64	$6.43	
R5F562N7ADLE#U0	384	64	$6.79	
R5F562N7BDBG#U0	384	64	$7.50	
R5F562N7BDFB#V0	384	64	$7.14	← too large
R5F562N7BDFP#V0	384	64	$6.79	
R5F562N7BDLE#U0	384	64	$7.14	
R5F562N8ADBG#U0	512	96	$7.63	
R5F562N8ADFB#V0	512	96	$7.26	← too large
R5F562N8ADFP#V0	512	96	$6.90	← Not enough I/O
R5F562N8ADLE#U0	512	96	$7.26	
R5F562N8BDBG#U0	512	96	$7.98	
R5F562N8BDFB#V0	512	96	$7.63	← too large
R5F562N8BDFP#V0	512	96	$7.26	← Not enough I/O
R5F562N8BDLE#U0	512	96	$7.63	

↑ Some Flash too small

RX62N/RX621 Group
RENESAS 32-Bit MCU

R01DS0052EJ0110
Rev.1.10
Feb 10, 2011

100 MHz 32-bit RX MCU with FPU, 165 DMIPS, up to 512-Kbyte Flash, Ethernet, USB 2.0 Full-Speed Host/Function/OTG, CAN, 12-bit ADC, TFT-LCD, RTC, up to 14 communication channels

Features

■32-bit RX CPU Core

- Delivers 165 DMIPS at a maximum operating frequency of 100 MHz
- Single Precision 32-bit IEEE-754 Floating Point
- Accumulator: 32 × 32 to 64-bit result, one instruction
- Mult/Divide Unit, 32 × 32 Multiply in one CPU clock for multiple instructions
- Interrupt response in as few as 5 CPU clock cycles
- CISC-Harvard Architecture with 5-stage pipeline
- Variable length instructions, ultra compact code
- Supports the Memory Protection Unit (MPU)
- Background JTAG debug plus high-speed trace

■Low Power Design and Architecture

- 2.7V to 3.6V operation from a single supply
- 480 µA/MHz Run Mode with all peripherals on
- Deep Software Standby Mode with RTC
- Four low power modes

■Main Flash Memory, no Wait-State

- 100 MHz operation, 10 nsec read cycle
- No wait states for read at full CPU speed
- 256K, 384K, 512K Byte size options
- For Instructions or Operands
- Programming from USB, SCI, JTAG, user code

■Data Flash Memory

- Up to 32K Bytes with 30K Erase Cycles
- Background Erase/Program does not stall CPU

■SRAM, no Wait-State

- 64K or 96K Byte size options
- For Operands or Instructions
- Back-up retention in Deep Software Standby Mode

■DMA

- Four fully programmable internal DMA channels
- Two EXDMA channels for external-to-external transfers
- Data Transfer Controller (DTC)

■Reset and Supply Management

- Power-On Reset (POR) monitor/generator
- Low Voltage Detect (LVD) with precision setting

■System Clocking with Clock Monitoring

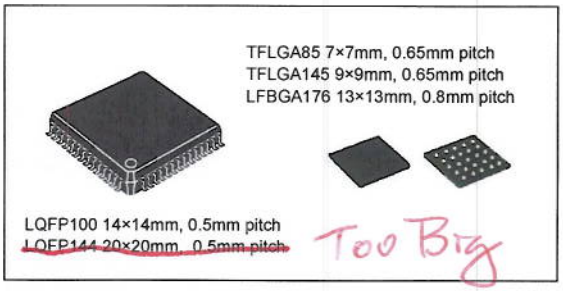
- External crystal, 8 MHz to 14 MHz to Internal PLL
- PLL source to system, USB, and Ethernet
- Internal 125 kHz LOCO for IWDT
- External crystal, 32 kHz for RTC

■Real Time Clock

- Full calendar function, BCD format

■Two Independent Watchdog Timers

- 125-kHz LOCO operation



■Up to 14 Communication Interfaces

- (2) USB 2.0 Full-Speed interfaces with PHY
- Supports Host/Function/OTG
  10 endpoints for types: Control, Interrupt, Bulk, Isochronous
- (1) Ethernet MAC 10/100 Mbps, Half or Full Duplex Supported.
  Dedicated DMA with 2-Kbyte transmit and receive FIFOs.
  RMII or MII interface to external PHY
- (1) CAN ISO11898-1, supports 32 mailboxes
- (6) SCI channels: Asynchronous, clock sync, smartcard, and 9-bit modes
- (2) I^2C interfaces up to 1M bps, SMBus support
- (2) RSPI

■External Address Space

- Eight CS areas (8 × 16 Mbytes)
- 128-Mbyte SDRAM area
- 8-/16-/32-bit bus space selectable for each area

■TFT-LCD up to WQVGA resolution

■Up to 20 Extended Function Timers

- (12) 16-bit MTU2
  Input capture, Output Compare, PWM output, phase count mode
- (4) 8-bit TMR
- (4) 16-bit CMT

■1-MHz ADC units with two combination choices

- 12-bit × 8 ch. unit with single sample/hold circuit
- or (2) 10-bit × 4 ch units each with a sample/hold circuit
- AD-converted value addition mode (12-bit A/D converter)

■10-bit DAC, 2 channels

■Up to 128 GPIO

- 5V tolerant, Open-Drain, Internal Pull-up

■Operation Temp

- –40°C to +85°C

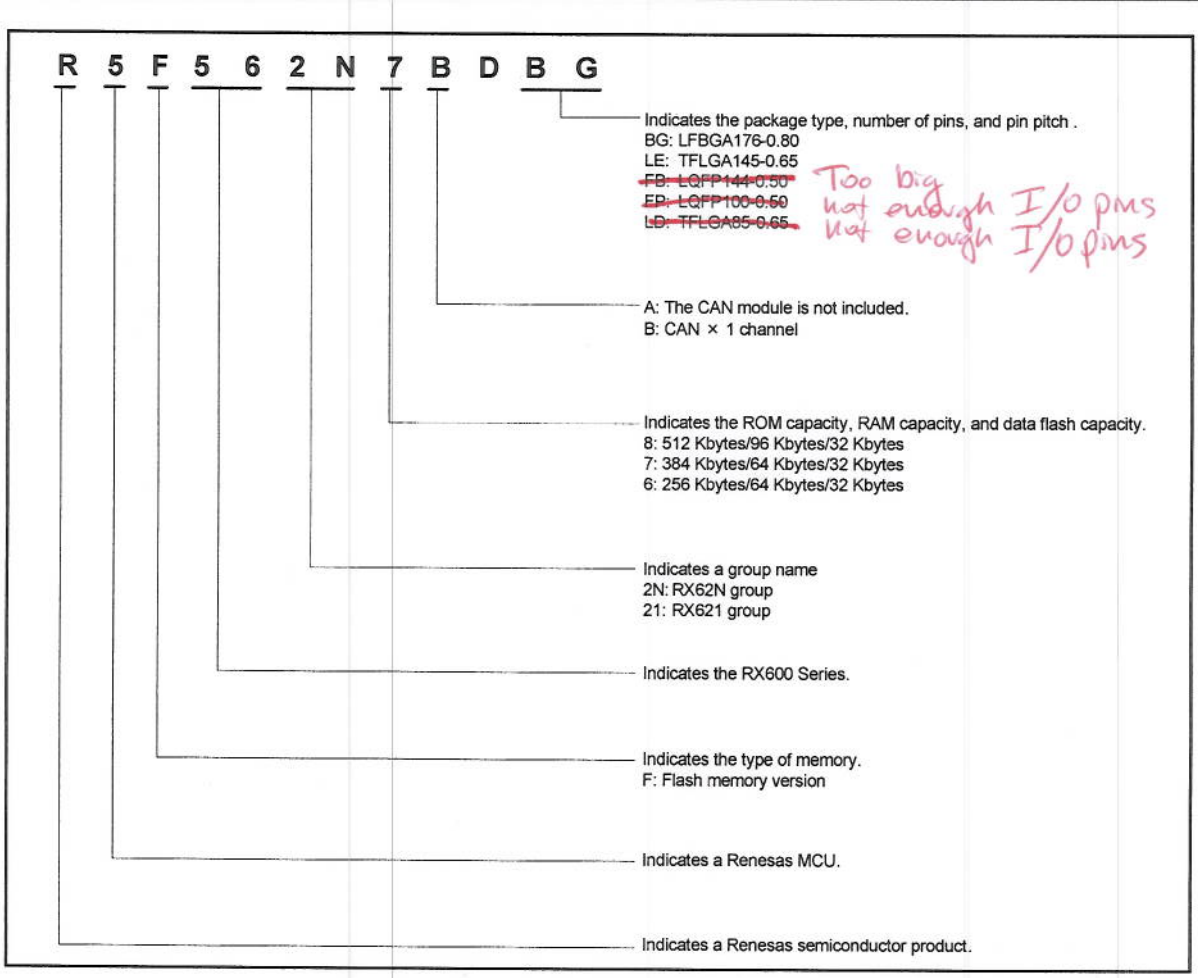


Figure 1.1 How to Read the Product Part No.

Table 1.1 Outline of Specifications (2 / 4)

Classification	Module/Function	Description
Interrupt	Interrupt control unit	· Peripheral function interrupts: 146 sources · External interrupts: 16 (pins IRQ0 to IRQ15) · Non-maskable interrupts: 3 (the NMI pin, oscillation stop detection interrupt, and voltage-monitoring interrupt) · Sixteen levels specifiable for the order of priority
	User break controller (as an optional function)	· Two breakpoint channels · Address breaks in fetch cycles are specifiable (enabling ROM correction)
External bus extension		· The external address space can be divided into nine areas (CS0 to CS7, SDCS), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS7), 128 Mbytes (SDCS) A chip-select signal (CS0# to CS7#, SDCS#) can be output for each area. Each area is specifiable as an 8-, 16-, or 32-bit bus space (however, only 176-pin versions support 32-bit bus spaces). The data arrangement in each area is selectable as little or big endian (only for data). · SDRAM interface connectable · Bus format: Separate buses · Wait control · Write buffer facility
DMA	DMA controller	· 4 channels · Three transfer modes: Normal transfer, repeat transfer, and block transfer · Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions
	EXDMA controller	· 2 channels · Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer · Single-address transfer enabled with the EDACK signal · Capable of direct data transfer to TFT LCD panels · Activation sources: Software trigger, external DMA requests (EDREQ), and interrupt requests from peripheral functions
	Data transfer controller	· Three transfer modes: Normal transfer, repeat transfer, and block transfer · Activation sources: Software trigger, external interrupts and interrupt requests from peripheral functions
I/O ports	Programmable I/O ports	· I/O ports for the 176-pin LFBGA/145-pin TFLGA/144-pin LQFP/100-pin LQFP/85-pin TFLGA · I/O pins: 126/103/103/72/58 · Input pins: 2/2/2/2/2 · Pull-up resistors: 56/44/44/40/28 · Open-drain outputs: 35/33/33/27/23 · 5-V tolerance: 11/11/11/7/6
Timers	Multi-function timer pulse unit	· (16 bits x 6 channels) x 2 units · Time bases for the 12 16-bit timer channels can be provided via up to 32 pulse-input/output lines and six pulse-input lines · Select from among eight counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. · Input capture function · 21 output compare/input capture registers · Pulse output mode · Complementary PWM output mode · Reset synchronous PWM mode · Phase-counting mode · Generation of triggers for A/D converter conversion
	Port output enable	· Controls the high-impedance state of the MTU's waveform output pins