An Ultra Low Power System Architecture for Sensor Network Applications

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Overview

- Introduction
- Sensor Network Applications
- System Design and Architecture
- Process Technology and Circuit Techniques
- Proof of Concept Results
- Conclusion
- Questions

Introduction

- Wireless Sensor Networks transform the way society interacts with the physical world.
- Proposed and deployed for applications-structural monitoring, habitat monitoring, emergency medical response etc
- Operating life time of the battery operated in WSN.
- Current deployment –Mica2
- Disadvantage-High power Consumption and limited operational life times.
- Overcome this limitation-Ultra Low Power device.

Introduction Contd….

- Paper outlines – design approach of system design from applications to circuits and process technology
- Low power
- Long life time
- Optimize the architecture for frequent repetitive behavior
- Features-Event driven computation, eliminate unnecessary operating system overhead.
- Long life time demands –fine grain power management.

Sensor Network Applications

- Study to understand computational needs of sensor network.
- Hardware requirements vary depending on projected
  - Life time
  - Computational complexity and
  - Communication needs of the deployment.
- Nodes complete data generation tasks such as
  - Talking to sensor samples,
  - Preparing messages containing data and
  - Sending radio messages.

System Design And Architecture

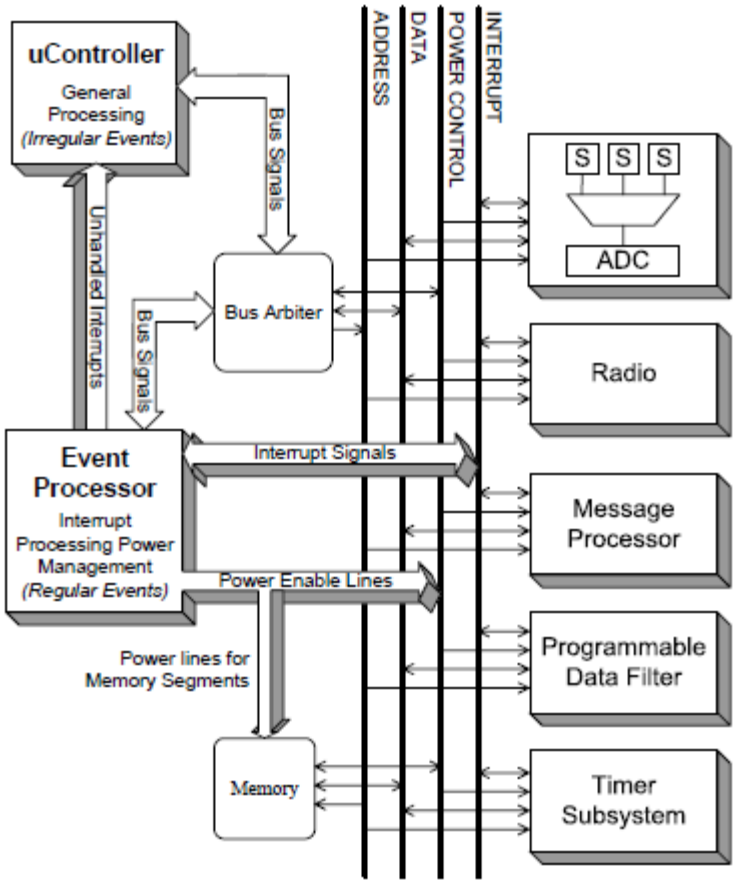


Figure 1. Block Diagram of System Architecture

System Design and Architecture Contd..

Architecture replaces the functionality of a general purpose microcontroller with an event driven system.

- *Event-Driven Computation: Eliminate unnecessary* event-processing overhead with an event-driven hardware platform.

- *Hardware Acceleration to Improve Performance and Power: Build a system composed of several components* that are optimized for specific tasks.

- *Exploiting Regularity of Operations within an Application:* Optimize the common-case behavior within an application.

System Design and Architecture Contd..

- *Optimization for a Particular Class of Applications:*

  To reduce power, while still providing general-purpose processing capability to enable broad functionality.

- *Modularity: architecture* that allows different sets of hardware components to be combined into a larger system targeting a particular application.

- *Fine-grain Power Management Based on Computational Requirements: Provide explicit programmer accessible* commands for fine-grain resource and power control.

System Components

- System Bus – Data Bus
  Interrupt Bus
  Power Control Lines
- Microcontroller- Irregular Programs such as
  System Initialization
  Reprogramming
- Event Processor-a programmable state machine designed to perform the repetitive task of interrupt handling

- Timer Subsystem- a set of four 16-bit timers. Timer is a counter that counts down to zero from a pre-configured value, and then generates an alarm event.

System Components

- Message Processor- Used for regular message processing tasks, including message preparation and routing

- Radio- Provides hardware support for tasks like

  Start symbol detection

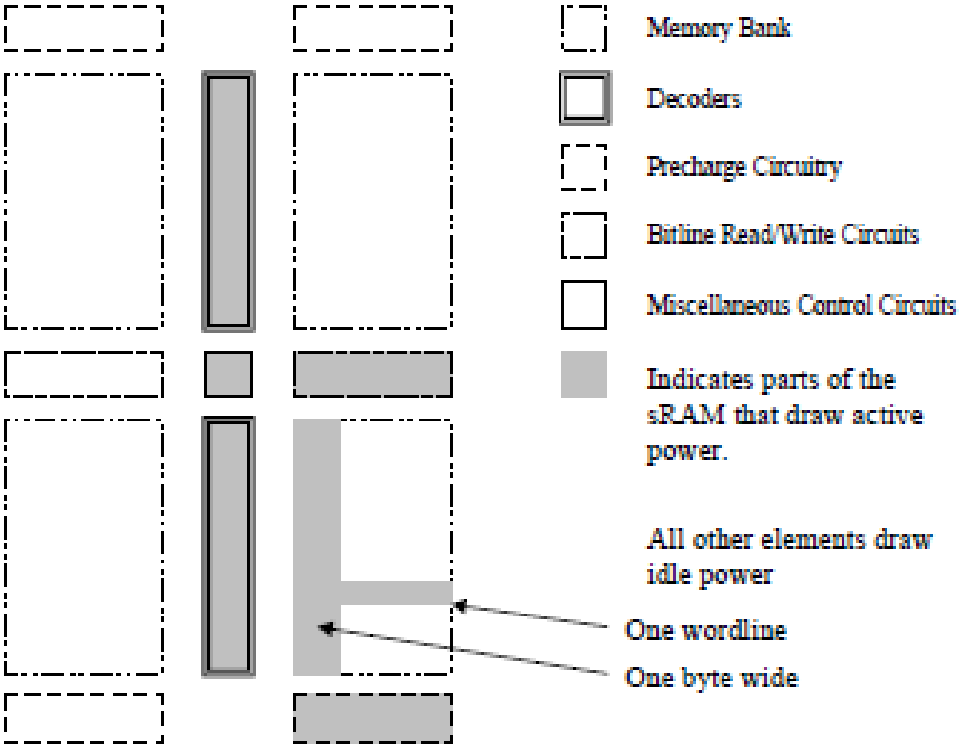
  Error detection etc.

Process Technology and Circuit Techniques

Circuit techniques and the choice of process technology can significantly impact the power consumed by the sensor nodes

Results of a process technology simulation study and the architecture and circuit design of a low-power SRAM.

Low Power Memory Design



Power Usage Characteristics of a 1KB SRAM

Proof of Concept Results

Performance Modeling –System C Simulator

- SystemC is a set of C/C++ libraries that is used to model high level architectural behavior
- Cycle-accurate simulator written in SystemC to characterize the cycle-level behavior of our architecture.

Test Application

Describe the four application versions according to the complexity added in each stage:

1. Periodically collect samples and transmit packets containing the samples.
2. Periodically collect samples and transmit packets containing the samples if it is above a certain threshold.

3. Receive and forward incoming messages from other sensor nodes.

4. Receive and handle incoming reconfiguration messages.

Measurement	Mica2	Our System	Speedup
Total send path w/out filter	1522	102	14.9
Total send path w/ filter	1532	127	12.1
Process regular message	429	165	2.6
Process irregular message			
Timer change	234	136	1.7
Threshold change	11	114	0.096
Units	Cycles	Cycles	×

Comparison of cycle count for the test application written on our architecture and on TinyOS for theMica Platform.

Conclusion

- Describes a holistic approach to the design of a wireless sensor network device.
- Describes- Selection of Process technology

  Circuit Design Considerations

  Novel System Architecture for Sensor Devices

Questions ?