Architecture Research and IC Design for Embedded Ultra – Micro Processor

-by
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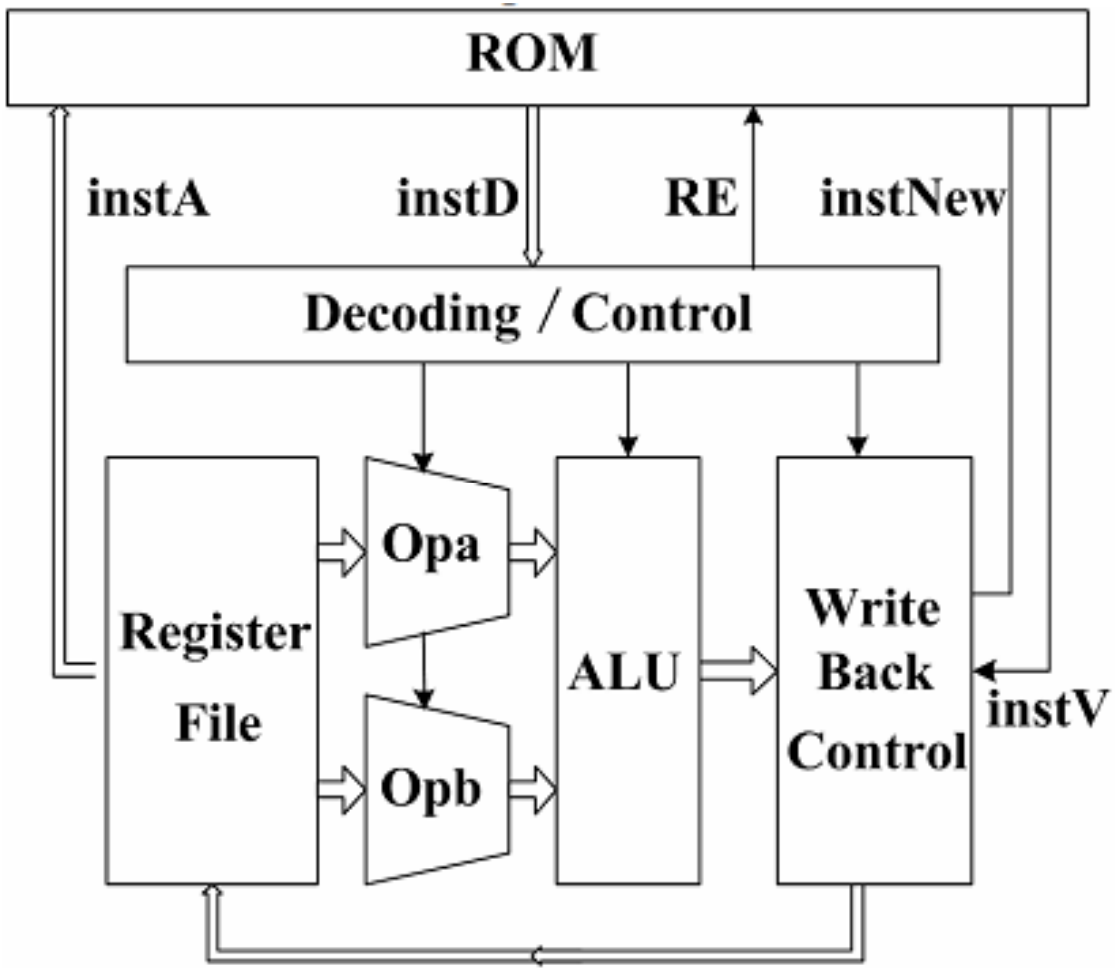
Introduction

Embedded System Design

- Simplex parallel combinational Circuit
  - ✓ High Speed, small circuit area and high performance – Advantage
  - ✓ Complex design needs, debugging – Disadvantage
- Use a general processor
  - ✓ Design based on processor is fast and easy to debug – Advantage
  - ✓ Area, less cost performance - Disadvantage

- Simplification without RAM or ROM access
  - ✓ Immediate and Register addressing modes are considered no access of memory in the Instruction set architecture level
- Registers are mapped as in / out ports
- 16 bit instruction encoding, sixteen 8 bit registers
- three instruction types: double-operand instruction, single-operand instruction and branch instruction.

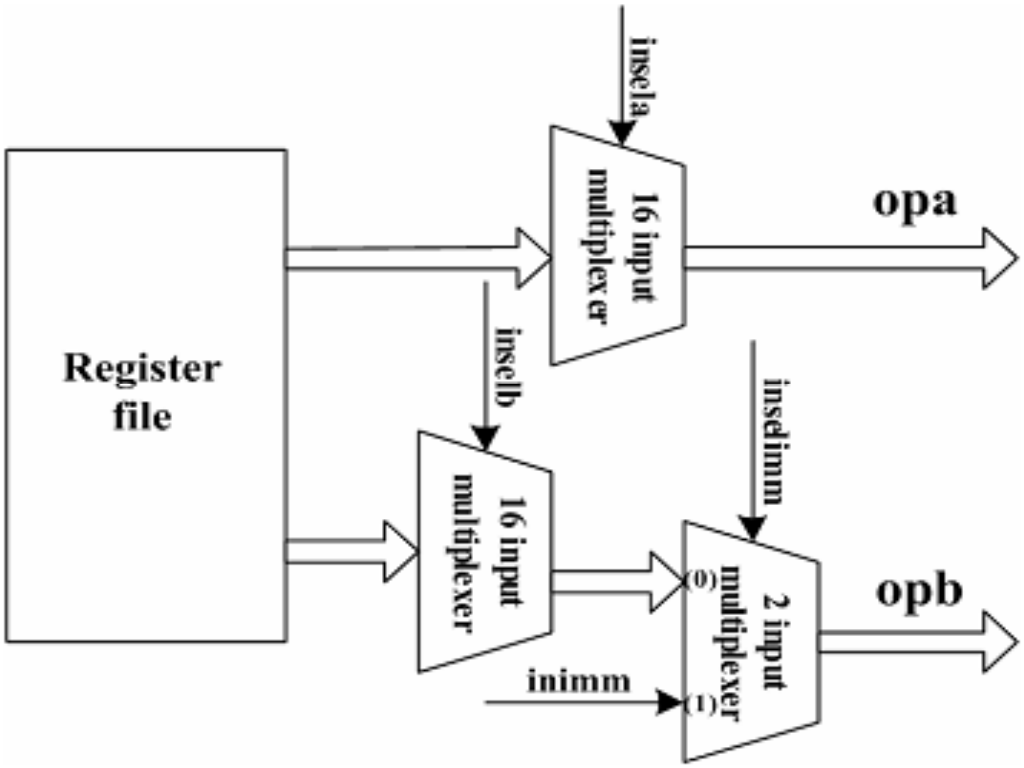
IC Design of UMP – General Architecture



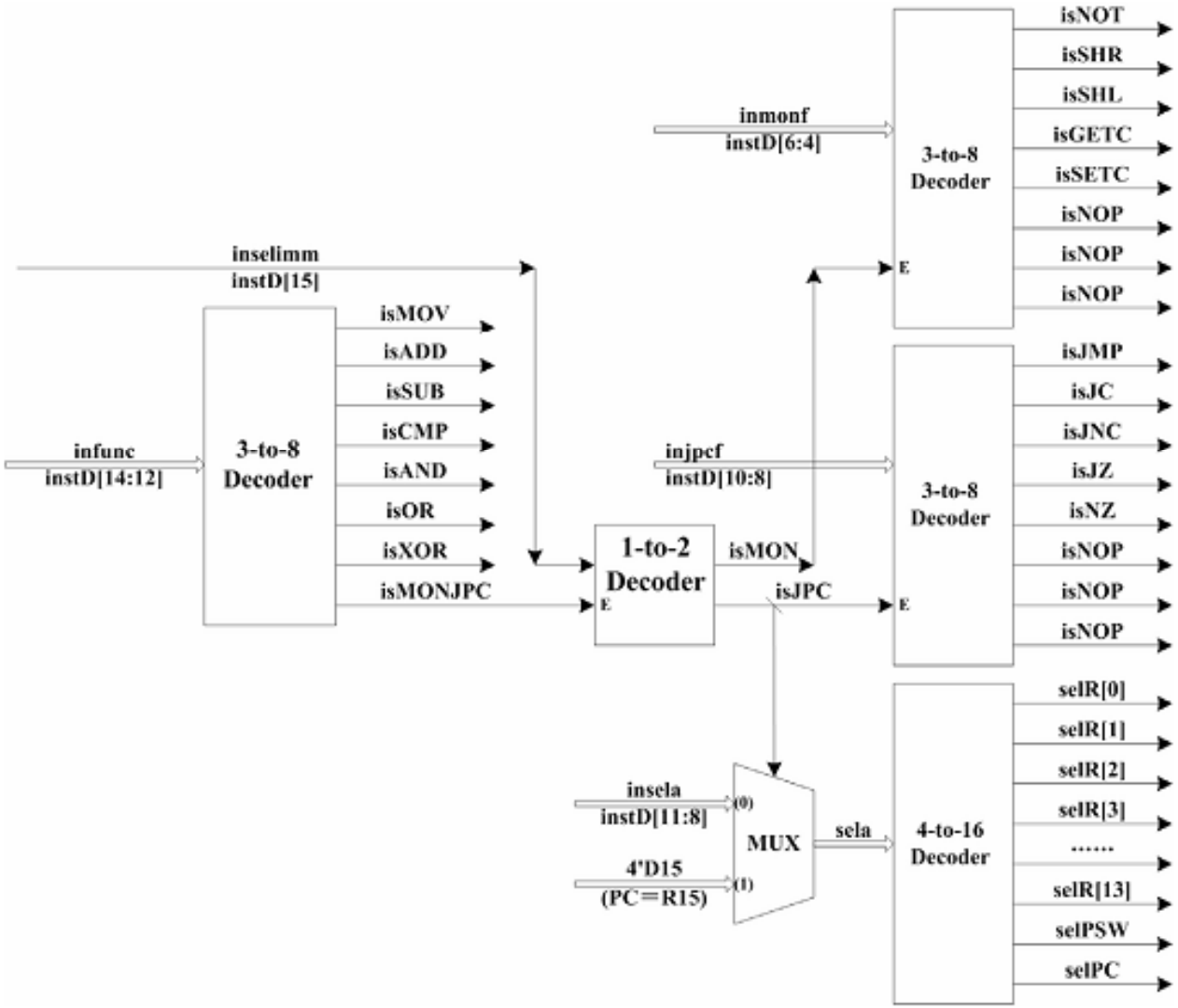
Instruction formats

Format	instD[15:0]															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1a	MOV/ADD/SUB/CMP/AND/OR/XOR Ra,Rb															
	inselimm	infunc			insela				inselb				xxxx			
	(0)	(000-110)			(0000-1111)				(0000-1111)							
1b	MOV/ADD/SUB/CMP/AND/OR/XOR Ra,#imm															
	inselimm	infunc			insela				inimm							
	(1)	(000-110)			(0000-1111)				(00H-FFH)							
2	NOT/SHR/SHL Ra || GETC/SETC Ra,n															
	inselimm	infunc			insela				x	inmonf			x	inoptn		
	(0)	(111)			(0000-1111)					(000-100)				(000-111)		
3	JMP/JC/JNC/JZ/JNZ #imm															
	inselimm	infunc			x	injpcf			inimm							
	(1)	(111)				(000-100)			(00H-FFH)							

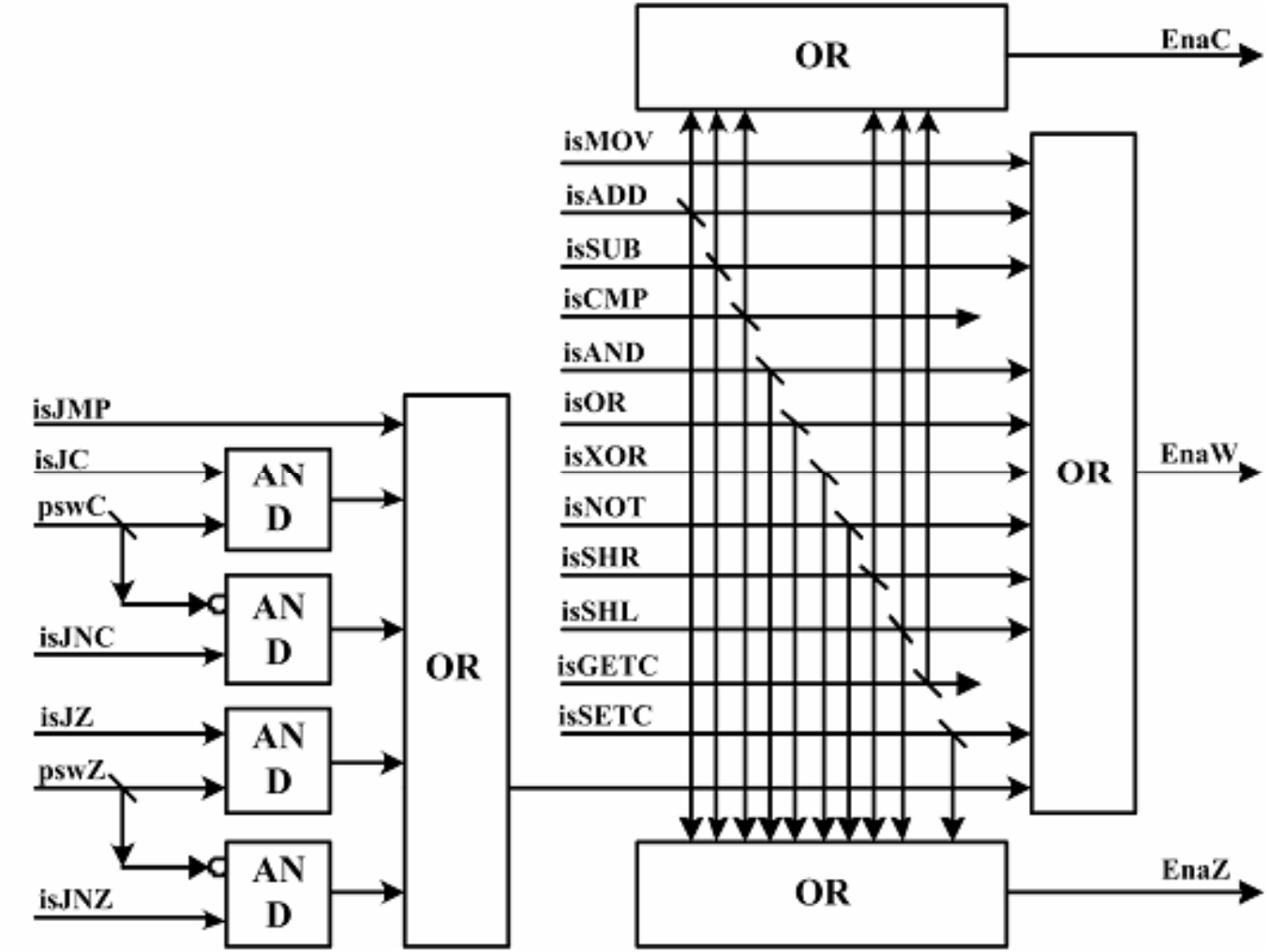
Operand Fetch Logic



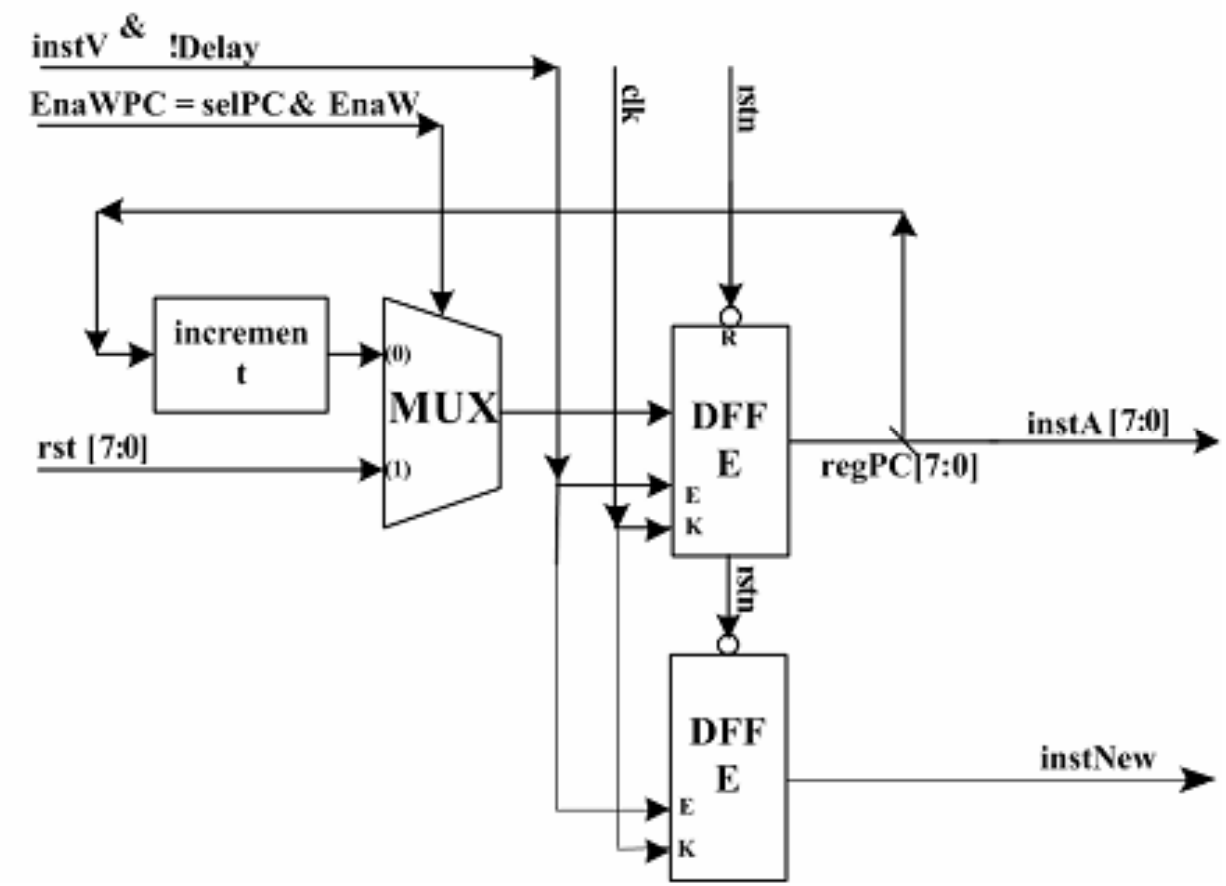
Instruction Decoding



Enable Logic



Write back


instV & !Delay
EnaWPC = selPC & EnaW
clk
rstn
incremen t
(0)
MUX
(1)
rst [7:0]
R
DFF E
E
K
instA [7:0]
regPC[7:0]
rstn
DFF E
E
K
instNew

Shoot Questions