An Embedded EEG Analyzing System Based on µC/os-II

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Agenda

- Background

- System Design

- Measurement Device

- Amplifier Design

- Software Design

- Task Configuration

- Data Structuring

- Filtered Data

- PC Software Design
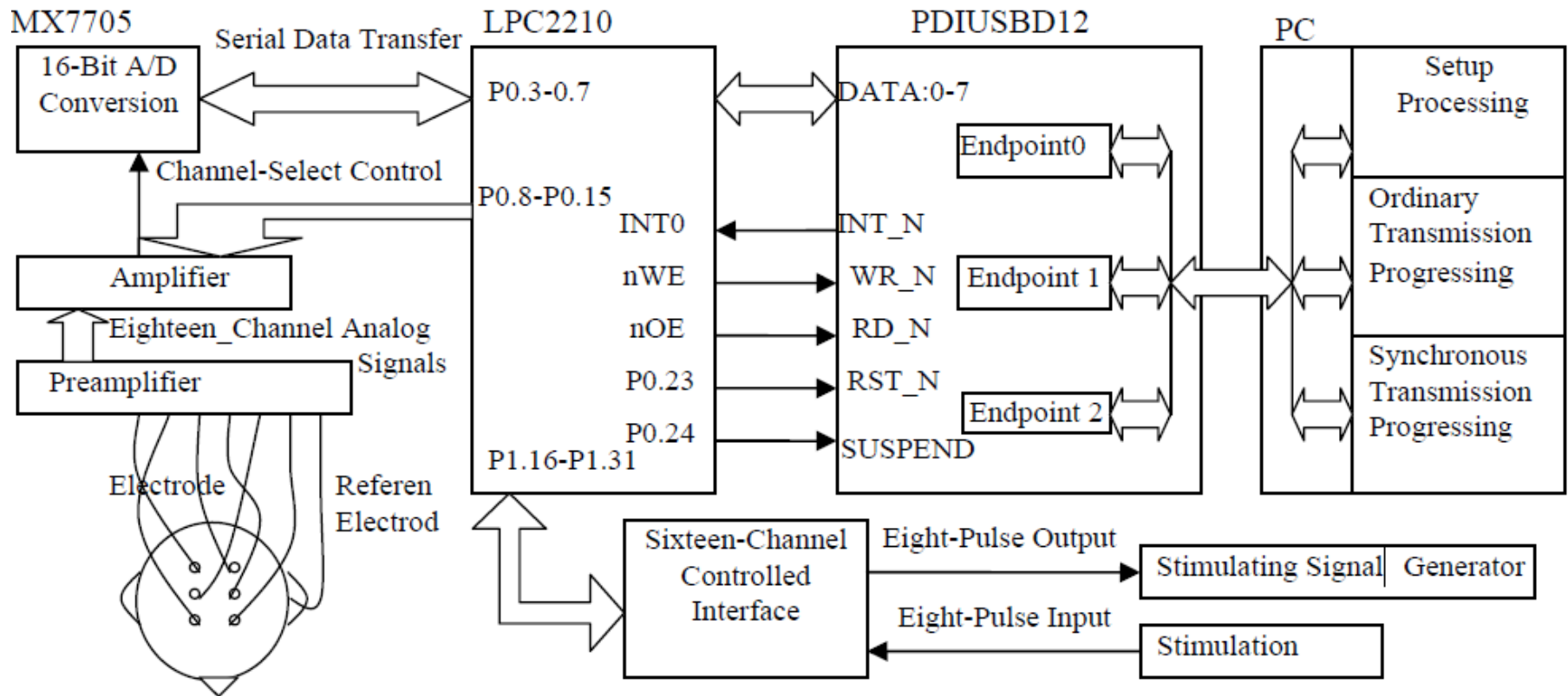
- Experiment

- Conclusions

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Background

- EEG systems traditionally bulky
- Can be used to detect seizures, monitor anesthesia, coma monitoring
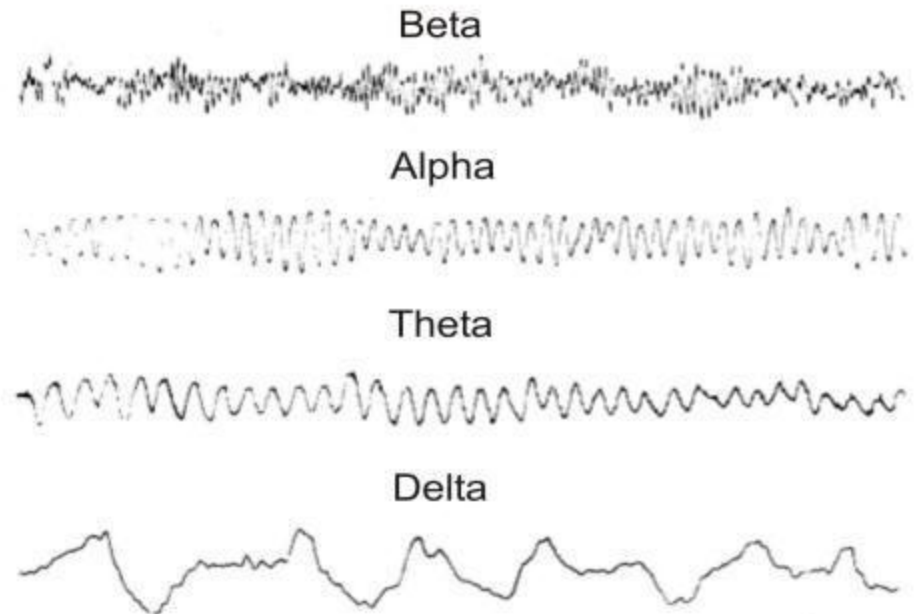
System Design

- ## Two main parts:
    - ### EEG measurement PC
    - ### EEG measurement device

Measurement Device

- Amplifier, filter, and A/D conversion before sent to ARM

- Processes event-related potentials (ERPs)

- ERP uploaded to PC

- Uses 8 channels to distinguish eight different simulations

- Synchronized signals of different simulations are recorded then all processed together.

Amplifier Design

- Signals generally in the tens of microvolts range
- Prevent noise while ensuring stability of signals
- MAX4197 used as the HPF with a cutoff frequency of 0.96Hz (adjustable)
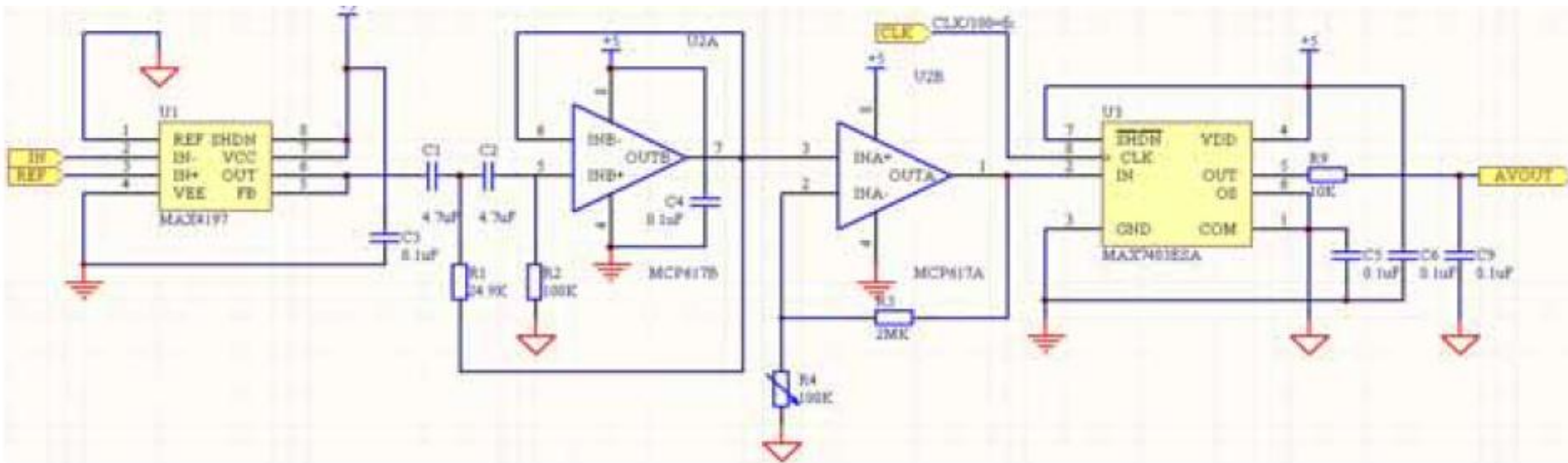- MAX7403 used as the LPF with range of 0.1Hz-10kHz

Fig. 2. Schemaic of Amplifier

Software Design

- Based on µC/os-II Real-Time Operating System
- Systems functions divided into five modules
  - Signal Acquisition
  - Data Preprocessing
  - Parameter Setting
  - Order Implementing
  - Data Transmission

- The RTOS establishes a task priority table and breaks down the processes into many smaller tasks

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Task Configuration

- Smaller tasks are prioritized into smaller system functions

- Configuration modes control the transmission

- Connected via USB to PC

TABLE I
THE LOGIC OF TASK

mailbox		
ordinary transmission task priority 5	scheduling task in μC/os-II kernel	parameter setting task order Implementing task Priority 4
synchronous data transmission task priority 1		signal acquisition task priority 2
data preprocessing task priority 3		

TABLE II
CONFIGURATION OF MODE 1

Num	Endpoint Index	Transmission	Endpoint Type	Direction	Bit
0	0	controlling output	acquiescence	output	16
	1	controlling input		input	16
1	2	ordinary output	ordinary	output	16
	3	Ordinary input	ordinary	input	16
2	4	synchronos output	Synchronization	output	128

Data Structuring

- There are 18 EEG channels to collect data with a speed of 1000 collections per second

- Data is stored in 18 small arrays corresponding with each channel as the Pre_Data

```
Typedef struct _PRE_DATA
{   uint    nDatahead;
    uint    nChannelNum;
    uint8   nChannel_1[3];

        ...........
    uint8   nChannel_18[3];
    uint8   nRespons
}PRE_DATA, *P_PRE_DATA
```

Filtered Data

- The Data is then filtered via STRU_DATA to encapsulate it

- Every encapsulation has 10 millisecond EEG data and the simulation signals

```
Typedef struct _DATA
{ int      nDatahead;
      int      nChannelNum;
      int      nDataNum;
      int      nChannel_1[N];
      ………….                    // N=10
      int      nChannel_18[N];
      short   nRespons [N]
}STRU_DATA, *P_STRU_DATA
```
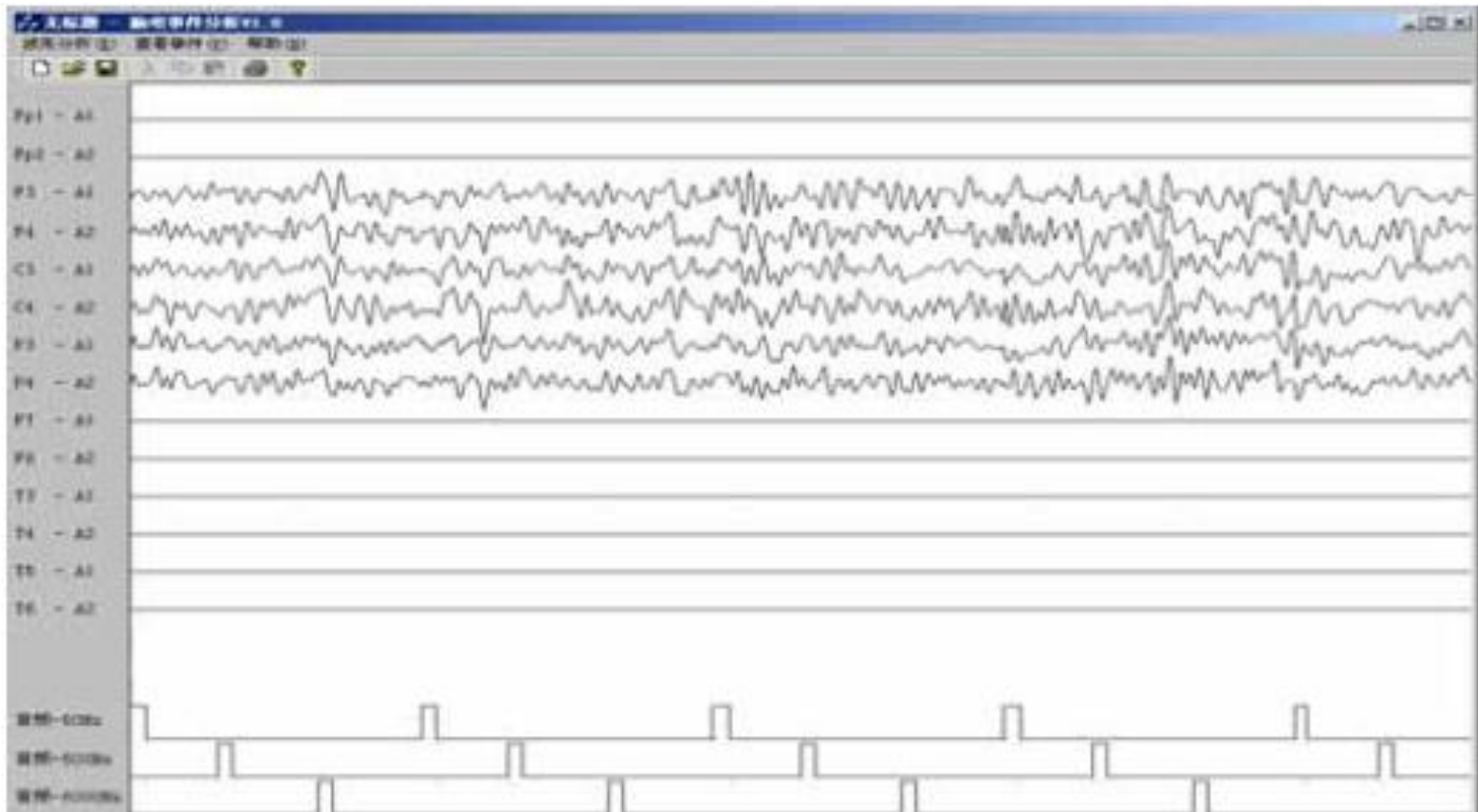
PC Software Design

- Function of PC is to provide a platform for the EEG data collection, display, and processing

- It is necessary to adjust cut-off frequency (15-120Hz) of filter for simulation signals
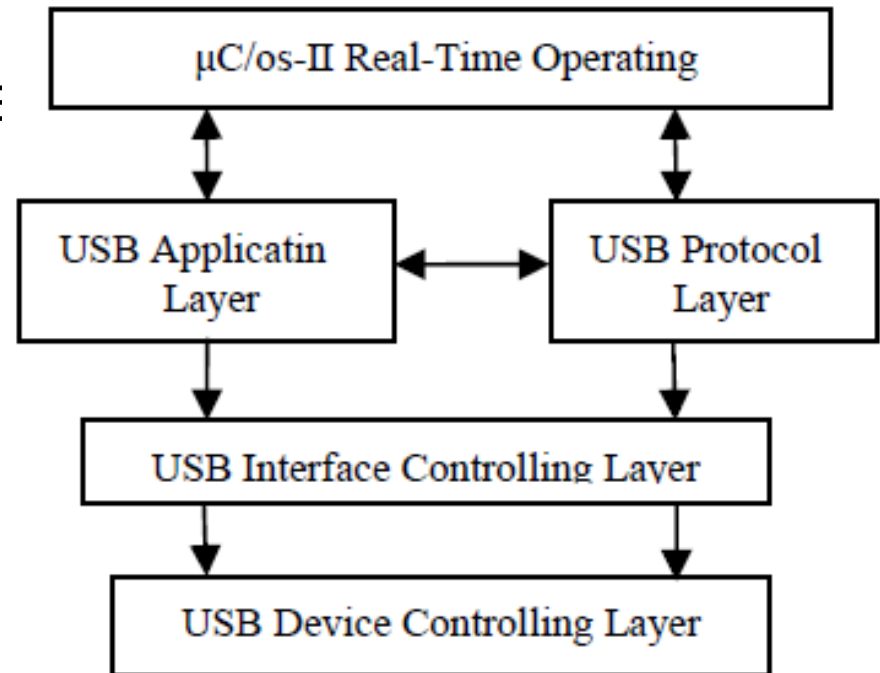
Data Acquisition Experiment

- EEG signals from 6 Channels
- PC received the signals from the ARM
- ER signals are considerably faint

Conclusion

- By processing and acquiring data on the ARM and making it compatible with a PC through USB the overall system size and power requirements have been drastically reduced.

- System expandable to 128 channels

- Moving forward:
  - Applications of signals
  - Show expandability with 128 channels (slowdowns?)

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