Hardware Multitasking in Dynamically Partially Reconfigurable FPGA-based Embedded Systems

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Dynamic Partial Reconfiguration

Certain FPGAs have a capability of being reconfigured during runtime.

- Static region:

  Area on FPGA which is loaded during power-up in the form of bitstream and not changed during runtime.

- Reconfigurable region:

  Area on FPGA which is reconfigured during runtime via a configuration port.

- Fast reconfiguration and preemption mechanism used to suspend or restore Hardware task execution.
- System implements priority based scheduling supporting preemptive and non-preemptive multitasking.

  Which task are we talking about in an FPGA system?

- Considering a system with different hardware configurations and we need to switch from one configuration to another.

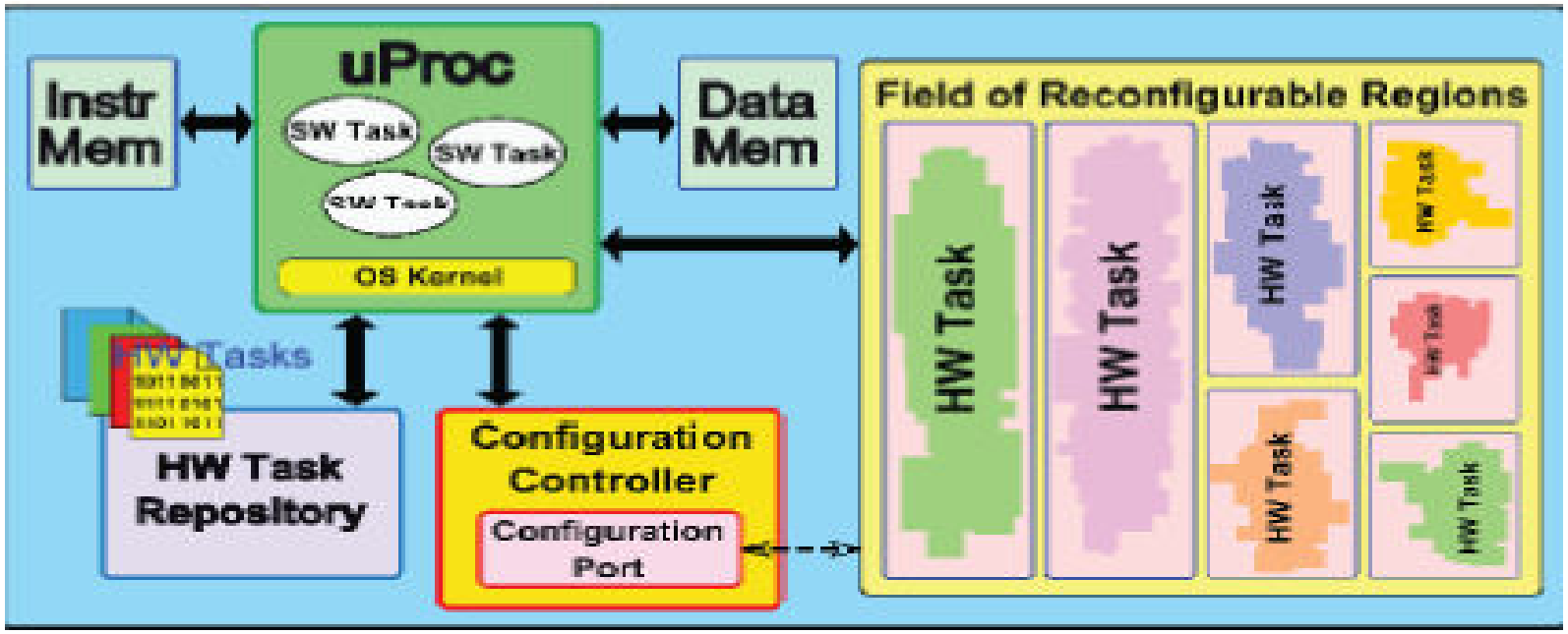
  1 Hardware Configuration =>1 Task

  Many Hardware Configuration =>Many Tasks

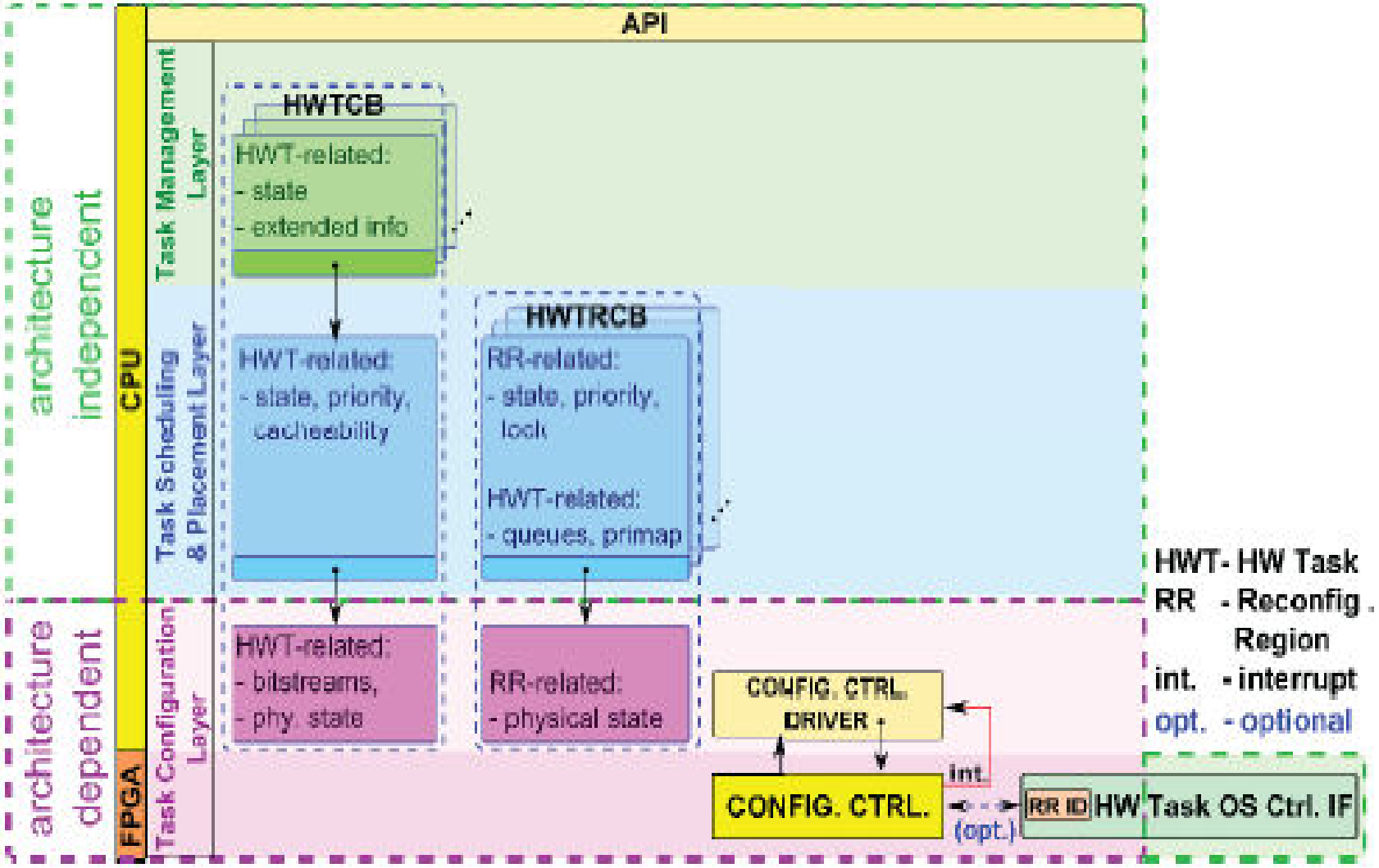
Example:

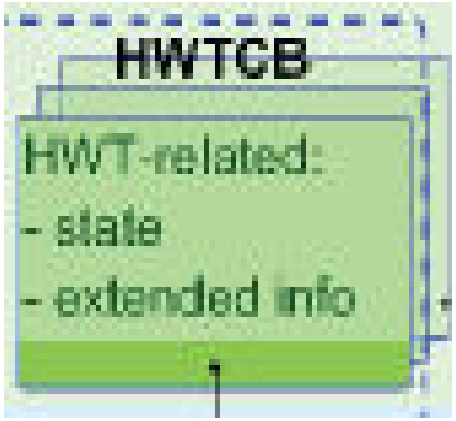
- To implement the scheduling of different tasks we need an OS which will run on a processor.

Below is the Reconfigurable Architecture model of the system.



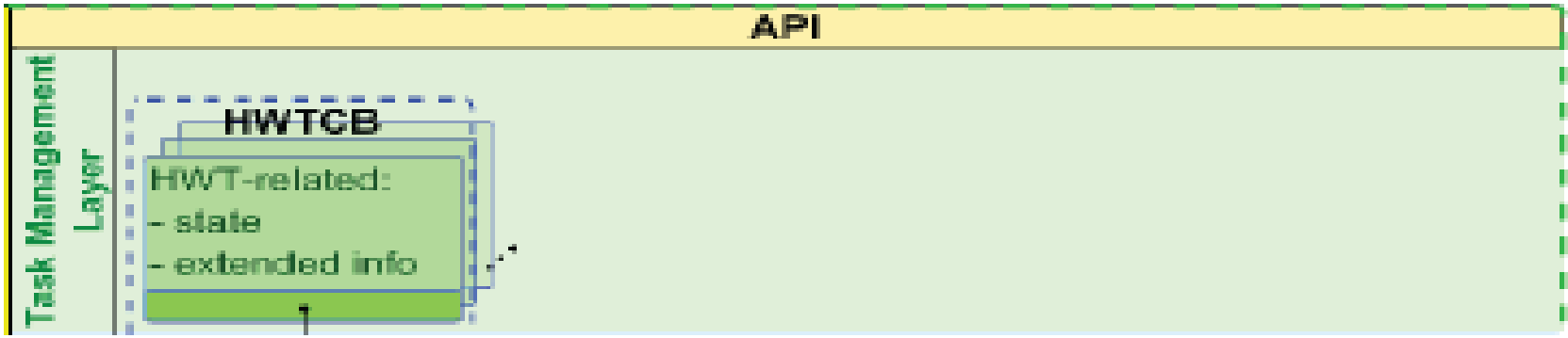
OS Extension Layers





- Hardware Task Control Block(HWTCB).
- Hardware Task Region Control Block.(HWTRCB)

  Hardware Task Repository is read from an external memory device (Compact Flash Card) during boot-up and used in initializing the HWTCB and HWTRCB.



- Task Management Layer:

  Easy use to API to the application programmer.

  Manage state of the Hardware Task.

- API:

  Calls for task activation, termination, inter task synchronization and task priority management.

- No calls for dynamic creation and deletion of tasks.
- With respect to this layer task can be in either runnable or non runnable state.

  Non-Runnable(Dormant,Wait,Suspended)

  Dormant state: Upon exit or termination.

  Wait / Suspended: Conditions for task execution are not met.

  Runnable: Task is ready to run.
- This layer is not aware if the given task is currently placed on the FPGA.

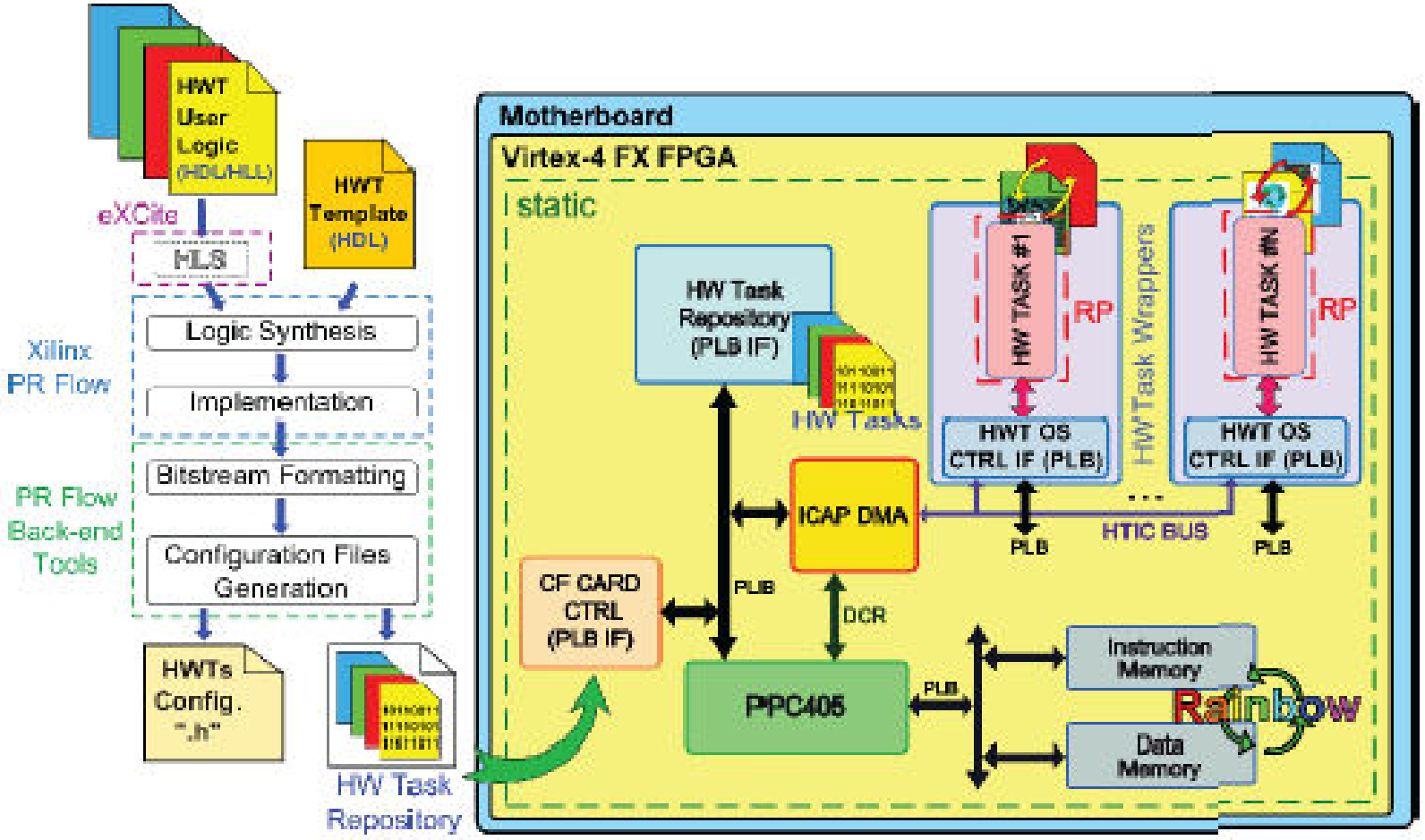
Task Scheduling and Placement Layer

- This layer makes the decision upon which task to allocate and start execution and is responsible for cacheability of tasks.
- Each Reconfigurable Region has an associated entry in the array of HWTRCB structures.

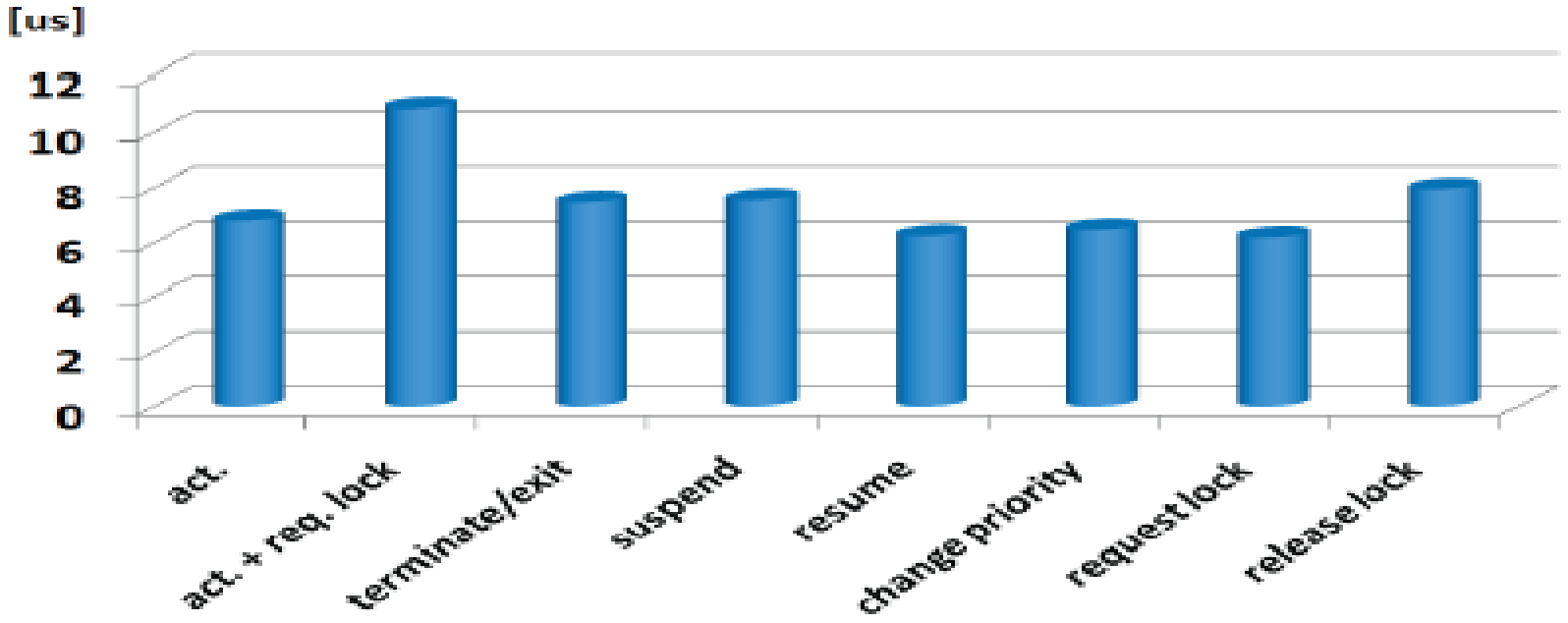
Task Configuration Layer

- This layer provides to the upper layer a programming interface used to control allocation, task management and RR's physical state.

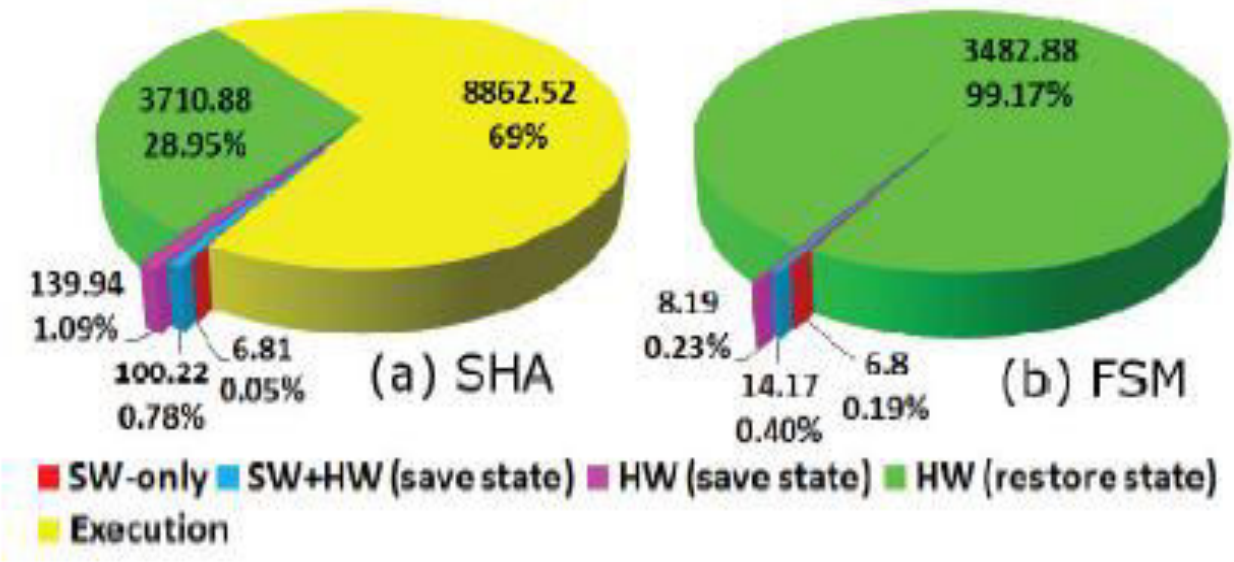
Hardware Platform and Design Flow



Experimental Results



Software Overhead of API calls.



Hardware Task Activation API call overhead.

References

- http://en.wikipedia.org/wiki/Partial_re-configuration
- 'Embedded System Design with Platform FPGA' by Ron Sass and Andrew G. Schmidt.
- http://www.altera.com/devices/fpga/stratix-fpgas/stratix-ii/stratix-ii-gx/features/transceiver/s2gx-dynamic-reconfiguration.html