HARDWARE DEVELOPMENT OF AN EMBEDDED WIRELESS EVALUATION BOARD

by

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ABSTRACT

ASSAD ANSARI. Hardware Development of an Embedded Wireless Evaluation board. (Under the direction of Dr. JAMES M. CONRAD)

The IEEE 802.15.4 standard specifies the physical (PHY) and media access layer (MAC) for simple, low-cost radio communication networks, offering low data rates and low energy consumption. A hardware platform implementing such a standard would form a good fit for applications that demand a strictly low power environment and a less demanding data rate. A platform to evaluate the behavior of the wireless protocol and analyze the current consumption will provide a better understanding of the standard and help in efficiently implementing the protocol, thus improving its use in domestic and industrial environments. This thesis work involves designing a simple platform to provide an empirical wireless measurement environment that can be extended to more complex network with several nodes. The evaluation board consists of the CHIPCON CC2420 low-cost RF transceiver designed specifically for low-power, low-voltage RF applications in the 2.4 GHz unlicensed ISM band. The board also contains an ATmega 128L microcontroller and two DS2740 coulomb counters to measure the power consumed by the microcontroller and the RF transceiver. A detailed design flow was formulated according to the hardware specifications and followed through out the design cycle.

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LIST OF ABBREVIATIONS

LR-WPAN	Low-Rate Wireless Personal Area Network
ISO	International Standard Organization
OSI	Open System Interconnection
PHY	Physical
ISM	Industrial Scientific Medical
WLAN	Wireless Local Area Networks
PER	Packet Error Rate
LQI	Link Quality Indication
DSSS	Direct Sequence Spread Spectrum
FFD	Fully Functional Device
RFD	Reduced Functional Device
CSMA-CA	Carrier Sense Multiple Access with Collision Avoidance
CRC	Cyclic Redundancy Check
MAC	Medium Access Control
ADC	Analog to Digital converter
ATmega 128L	AVR ATmega 128L microcontroller
CC2420	CHIPCON CC2420 RF transceiver
CCA	Clear Channel Assessment
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
CS	Chip Select
DAC	Digital-to-Analog Converter

DQ	Data Input/Output
DS2740	MAXIM DS2740 Coulomb Counter
EEPROM	Electrically Erasable Programmable Read only Memory
FIFO	First In, First Out
I/O	Input/Output
IF	Intermediate Frequency
IS1	Current-Sense Input
ESD	Electro Static Discharge
JTAG	Joint Test Action Group
LNA	Low Noise Amplifier
MPDU	MAC Protocol Data Unit
OVD	1-Wire Bus Speed Select
PA	Power Amplifier
PIO	Programmable I/O Pin
PWM	Pulse Width Modulation
RISC	Reduced Instruction Set Computer
RSSI	Received Signal Strength Indication
RTC	Real Time Counter
RXFIFO	Receive FIFO
SCLK	System Clock
SFD	Start of Frame Delimiter
SI	System In
SNS	Sense Resistor Input

SO	System Out
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TXFIFO	Transmit FIFO
VDD	Power-Supply Input (2.7V to 5.5V)
VSS	Device Ground, Current-Sense Resistor Return

CHAPTER 1: INTRODUCTION

The IEEE 802.15.4 standard specifies the physical (PHY) and media access layer (MAC) for simple, low-cost radio communication networks. These networks offer low data rates and low energy consumption. The purpose of the IEEE 802.15.4 specification is to provide a standard for ultra-low complexity, ultra-low cost, ultra-low power consumption, and low data rate wireless connectivity among inexpensive devices [3].

The IEEE 802.15.4 provides a reliable communication protocol and defines both a star and a peer-to-peer network topology. Two device types are possible: a full-function device (FFD) and a reduced-function device (RFD). A FFD device is capable of serving as the network coordinator since it implements the complete protocol stack, while a RFD is a simpler device with a minimal protocol stack implementation. Transmission distance is expected to range from 10 to 75 meters, depending on output power and the surrounding environment. Transmission can be optionally encrypted using Advanced Encryption System (AES) which is a functionality provided by IEEE 802.15.4. In order to provide flexibility for a range of applications, IEEE 802.15.4 operates in three frequency bands at different rates, offering flexibility to a range of applications [3].

1.1 Physical Layer

The main responsibility of the physical layer (PHY) is interacting with and controlling the radio transceiver. The layer also measures the energy level within the current channel and provides link quality indication (LQI) for received packets. Before sending packets over the air, PHY performs a CCA (Clear Channel Assessment) to

identify if the channel is busy. PHY is responsible for transmitting and receiving the packets on the correct frequency. The physical layer can operate in three different frequency bands at different rates, as summarized in Table 1. Devices not operating in 2.4 GHz band are required to operate in both 868 MHz and 902 MHz frequency band [7].

Frequency band (MHz)	Bit rate (kbps)	Number of Channels
868 – 868.6	20	1
902 – 928	40	10
2400 – 2483.5	250	16

TABLE 1: Frequency Bands and Data Rates

1.2 Media Access Layer (MAC)

The MAC is responsible for generating and synchronizing to the network beacons. The layer provides PAN association and disassociation, and provides a reliable link between two devices. It also offers an optional security for the MAC layer and maintains a GTS (Guaranteed Time Slot) mechanism for devices that require a constant rate and fixed delays. The MAC layer supports creation of two types of network topologies: star topology and peer-to-peer topology. In the star topology, all communication is controlled by the PAN coordinator. Any full-function device (FFD) can create its own network by becoming a PAN coordinator. The peer-to-peer topology allows more complex communication scenarios. Any FFD device might communicate with any other FFD device. It is possible to implement routing protocols in this topology. Reduced-function devices (RFD) might also participate in the network, but only as peripheral devices. They cannot relay packets and participate in routing mechanisms. Simply defining a PHY and a

MAC does not guarantee that different devices will be able to talk to each other. A scenario such as this demands a standard protocol. The ZigBee alliance was formed to define and develop the upper layers of network in conformance with the IEEE Std. 802.15.4 [7].

1.3 Motivation

The Embedded 802.15.4 Evaluation Board of this research effort has an Atmel ATmega 128L microcontroller with 128-Kbytes of self-programming Flash Program Memory, 4-Kbytes of SRAM, 4-Kbytes of EEPROM, a JTAG interface for on-chip-debug and an ISP interface. The board also has a serial interface for serial communications. There is a Coulomb Counter (DS2740) interfaced with the microcontroller and the RF transceiver to measure the power consumed by both of them independently. The RF section features a CHIPCON CC2420 RF transceiver compliant with IEEE 802.15.4 standard. The unused port pins on the microcontroller are provided on headers that can be used later for interfacing sensors or debugging purposes. The SPI interface pins between the microcontroller and the RF transceiver are also provided on headers for debugging software.

There are several 802.15.4 evaluation boards available in the market. However, a customized board to observe and analyze the power consumption during different stages of operation is not available. Any observation that can contribute to building efficient network would prove to be a valuable asset.

The manufacturing cost was also a major factor in building the board from scratch. This board provides an ideal platform for students to develop simple wireless

applications. In the future, firmware can be developed to integrate similar boards under a single network.

1.4 Current Work in this Area

IEEE 802.15.4 employs the 2.4 GHz Industrial, Scientific, Medical (ISM) band for its operation, which is also used by other IEEE 802 standards. Due to collocation of technologies, coexistence becomes a major area of research. The IEEE 802.15.4 standard can be used with sensors that control lights or alarms, wall switches that can be moved at will, wireless computer peripherals, controllers for interactive toys, smart tags, badges, inventory tracking devices and Automatic Meter Reading systems [6, 10].

1.5 Organization of Thesis

The thesis is organized in 7 major sections. Chapter 1 provides the aim, background and motivation behind the thesis. Chapter 2 specifies the functional requirements of the board and the choice of the components made depending upon the functional requirements. Chapter 3 gives a detailed description of the hardware components present on the board. Chapter 4 describes the interfacing techniques implemented for different on board components. Chapter 5 gives an introduction to OrCAD and the steps followed in Capture CIS to complete the schematic design. Chapter 6 discusses the Layout design and the steps followed in Layout plus to finish the PCB design. Chapter 7 includes the conclusion and discusses future areas of research.

CHAPTER 2: REQUIREMENTS AND SPECIFICATIONS

2.1 Requirements of the Board

The hardware requirements of the board were decided according to the functional requirements of the board. The cost of the board was also kept in mind when determining the hardware requirements. The requirements of the board were as follows:

- The board should have a microcontroller with enough internal memory to ensure communications and to run a simple application.
- The board should have a JTAG connection header for on-chip debug support and programming of flash, EEPROM, fuses, and lock bits through the JTAG interface.
- The board should have an ISP connector for in system programming.
- The board should have a low cost RF transceiver for transmitting and receiving data in IEEE 802.15.4 format.
- The board should only have a SMA connector for an external antenna.
- The board should have a device for measurement of the current consumed by the microcontroller and RF transceiver.
- The board should have two power supply inputs.
- The board should have two voltage regulators that should regulate the voltage from the two power supplies.
- There should be a RS-232 serial port for communications with the microcontroller.

- There should be an onboard header so that it can be used during testing.
- There should be a header for expansion of the hardware in future.
- The board should be two layers with copper pour for ground of the RF section.
- The board should be no larger than 3" X 2.5".
- All passive components should be of size 0603.
- All parts should be surface mount and all testing points should be through holes.
- Three LEDs should be available on the board for debugging purposes; these LEDs can be disabled by the programmer such that they draw no power.
- There should be two switches one for reset and one for debugging purposes.

2.2 Choice of Components

The microcontroller chosen for the application was the Atmel ATmega 128L. The reason for choosing ATmega 128L was its internal memory. It has 128 Kbytes of in-system programmable flash, 4 Kbytes of EEPROM and 4 Kbytes of SRAM. Therefore, no external memory was required as 128 Kbytes of in-system programmable flash is enough for the complete IEEE 802.15.4 stack. Absence of an external memory device helped in reducing the size and complexity of the embedded wireless evaluation board. The ATmega 128L provides various power management and sleep modes allowing the user to modify the power consumption to the application's requirements. The power management modes are:

1. **Idle mode:** In the idle mode the CPU is stopped but the SPI, USART, Analog Comparator, ADC, two wire serial interface, Timers/counters, watchdog timer and the interrupt system continue operating. This mode basically stops the CPU clock and the flash clock. It allows the microcontroller to wake up from externally

triggered interrupts as well as internal interrupts such as timer overflow and USART transmit complete.

2. **ADC noise reduction mode:** In the idle mode the CPU is stopped but the ADC, two wire serial interface, timers/counter0, and the watchdog timer continue operating. This mode basically stops the CPU clock, I/O clock and the flash clock while allowing other clocks to run. This improves the noise environment for the ADC, enabling higher resolutions. If the ADC is enabled a conversion starts automatically when this mode is entered.
3. **Power down mode:** In this mode the external crystal oscillator is stopped while the external interrupts, the two wire serial interface and the watchdog continue operating. This sleep mode basically halts all generated clocks allowing operation of asynchronous modules only.
4. **Power save mode:** This mode is the same as the power down mode with one exception if Timer/Counter0 is clocked by an asynchronous source. The device can wake up from timer overflow or output compare event from timer/counter0. This sleep mode basically halts all clocks, except the asynchronous clock allowing operation of asynchronous modules, including timer/counter0 if clocked asynchronously.
5. **Standby mode:** In this mode the external crystal/resonator option is selected. This mode is same as the power down mode with the exception that the oscillator is kept running. From the standby mode the microcontroller wakes up in just six clock cycles.

6. **Extended standby mode:** In this mode the external crystal/resonator option is selected. This mode is same as the power save mode with the exception that the oscillator is kept running. From the extended standby mode the microcontroller wakes up in just six clock cycles.

Another important feature of the Atmega 128L is its compliance with IEEE standard 1149.1 JTAG interface. The JTAG interface gives access to the on chip debug system and can be used to download firmware to the Atmega 128L. Firmware can also be downloaded to the Atmega 128L using the in system programmable interface called the ISP interface.

The CHIPCON CC2420 was chosen as the RF transceiver. It is a true single-chip 2.4 GHz IEEE 802.15.4 compliant RF transceiver with baseband modem and MAC support. It operates at a supply voltage of 2.1 – 3.6 V if an external voltage regulator is used and 1.6 – 2.0 V if the internal voltage regulator is used. It consumes very low current. The current consumption in receive mode is 19.7 mA and in transmit mode it is 17.4 mA. The current consumption when the CC2420 is not transmitting or receiving is just 1 μA. It requires very few external components and no RF switch/filter is required at the output. It also provides useful features such as packet handling, data buffering, burst transmissions, data authentication, data encryption, clear channel assessment, energy detection, received signal strength indication (RSSI), link quality indication (LQI) and packet timing information. These features reduce the load on the host microcontroller and allow CC2420 to be interfaced with low cost microcontrollers.

The Maxim DS2740, a high precision coulomb counter, was selected to monitor the current consumption of the Atmega 128L and CC2420. It measures current bi-

directionally over a dynamic range of 15 or 13 bits. It consumes 65 μA current in active mode and 1 μA in sleep mode. On the board designed, the DS2740 with 13 bits was used because it's four times faster than the device with 15 bits. Its measures current by sensing voltage drop across a low value current sense resistor. The voltage sense range is 51.2 mV. It has a voltage resolution of 6.25 μV LSB. The current resolution is 312 μA LSB and dynamic range is ±2.56A. A more detailed description of DS2740 specifications is given in Chapter 3.

MIC5209-3.3BS was used as the voltage regulator to regulate the voltage from the two power supplies. This voltage regulator was specially designed for battery-powered devices. It features low ground current to increase the battery life. It also has features such as reverse battery protection, current limiting, over temperature shutdown, ultra low-noise capability and is available in thermal efficient packaging. MAX3243, which is the RS232 line driver/receiver, was selected to serve as the interface between the microcontroller and the serial port. It has an important mode called auto power shut down. In this mode if it does not receive any valid signal at its receiver it shuts down its drivers and the supply current to the chip is just 1 μA.

CHAPTER 3: HARDWARE DESCRIPTION

3.1 Description of Hardware

This section gives a detailed description and features of the hardware components used on the embedded 802.1.5.4 evaluation board.

3.1.1 Overview of CHIPCON CC2420

The CHIPCON CC2420 is a single-chip 2.4 GHz IEEE 802.15.4 compliant RF transceiver designed for low-power and low-voltage wireless applications. The CC2420 includes a digital direct sequence spread spectrum base band modem providing a spreading gain of 9 dB and an effective data rate of 250 kbps. The CC2420 is a low-cost, highly integrated solution for robust wireless communication in the 2.4 GHz unlicensed ISM band. The RF transceiver also provides extensive hardware support for packet handling, data buffering, burst transmissions, data encryption, data authentication, clear channel assessment, link quality indication and packet timing information. These features reduce the load on the host controller and allow the CC2420 to interface with low-cost microcontrollers. The configuration interface and transmit / receive FIFOs of the CC2420 are accessed via an SPI interface. In a typical application the CC2420 will be used together with a microcontroller and the necessary passive and active components.

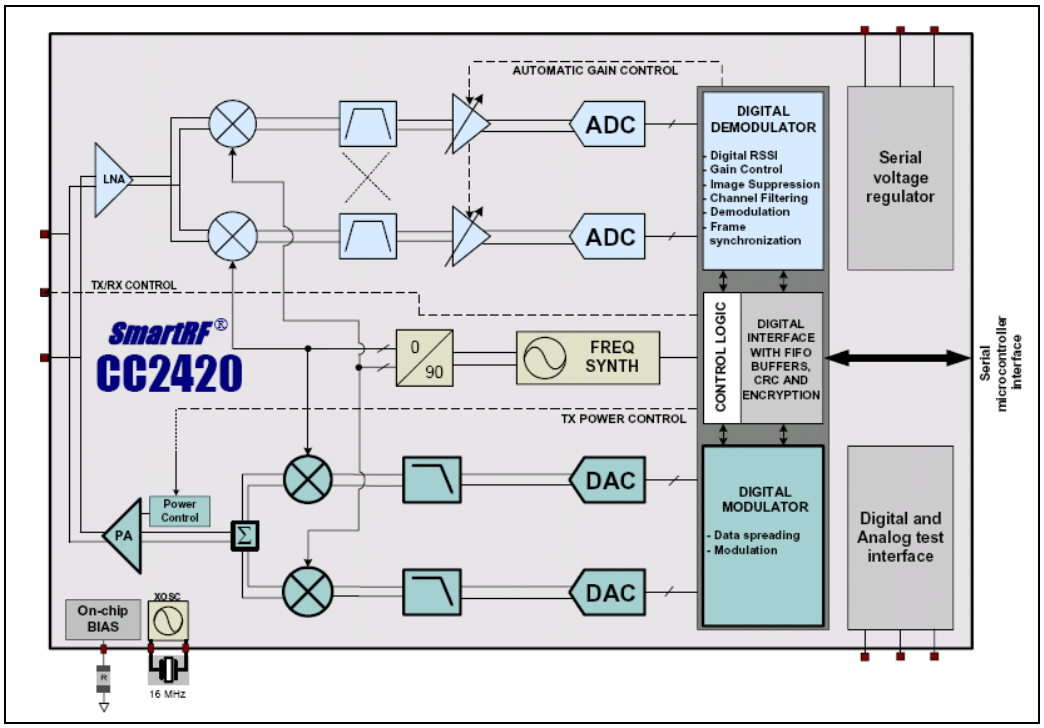

FIGURE 1: CC2420 Simplified Block diagram [2, p16]

Figure 1 illustrates a simplified block diagram of the CC2420, which features a low-IF receiver. The received RF signal is amplified by a low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF (2 MHz), the complex I/Q signal is filtered and amplified, and then digitized by the ADCs. Automatic gain control, final channel filtering, de-spreading, symbol correlation and byte synchronization are performed digitally. The SFD pin goes high when a start of frame delimiter has been detected. The CC2420 buffers the received data in a 128 byte receive FIFO. The user may read the FIFO through an SPI interface. Cyclic Redundancy Check bytes are verified in the hardware. RSSI and correlation values are appended to the frame. CCA is available on a pin in receive mode. Serial (unbuffered) data modes are also available for test purposes.

The CC2420 transmitter is based on direct up-conversion. The data is buffered in a 128 byte transmit FIFO (separate from the receive FIFO). The preamble and start of frame delimiter are generated by hardware. Each symbol (4 bits) is spread using the IEEE 802.15.4 spreading sequence to 32 chips and output to the digital-to-analog converters (DACs). An analog low-pass filter passes the signal to the quadrature (I and Q) up-conversion mixers. The RF signal is amplified in the power amplifier (PA) and fed to the antenna.

3.1.2 Overview of ATMEGA 128L

The ATmega 128L is a low-power CMOS 8-bit microcontroller based on the AVR Enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega 128L achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed. The AVR core features 32 general purpose working registers which are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers [1].

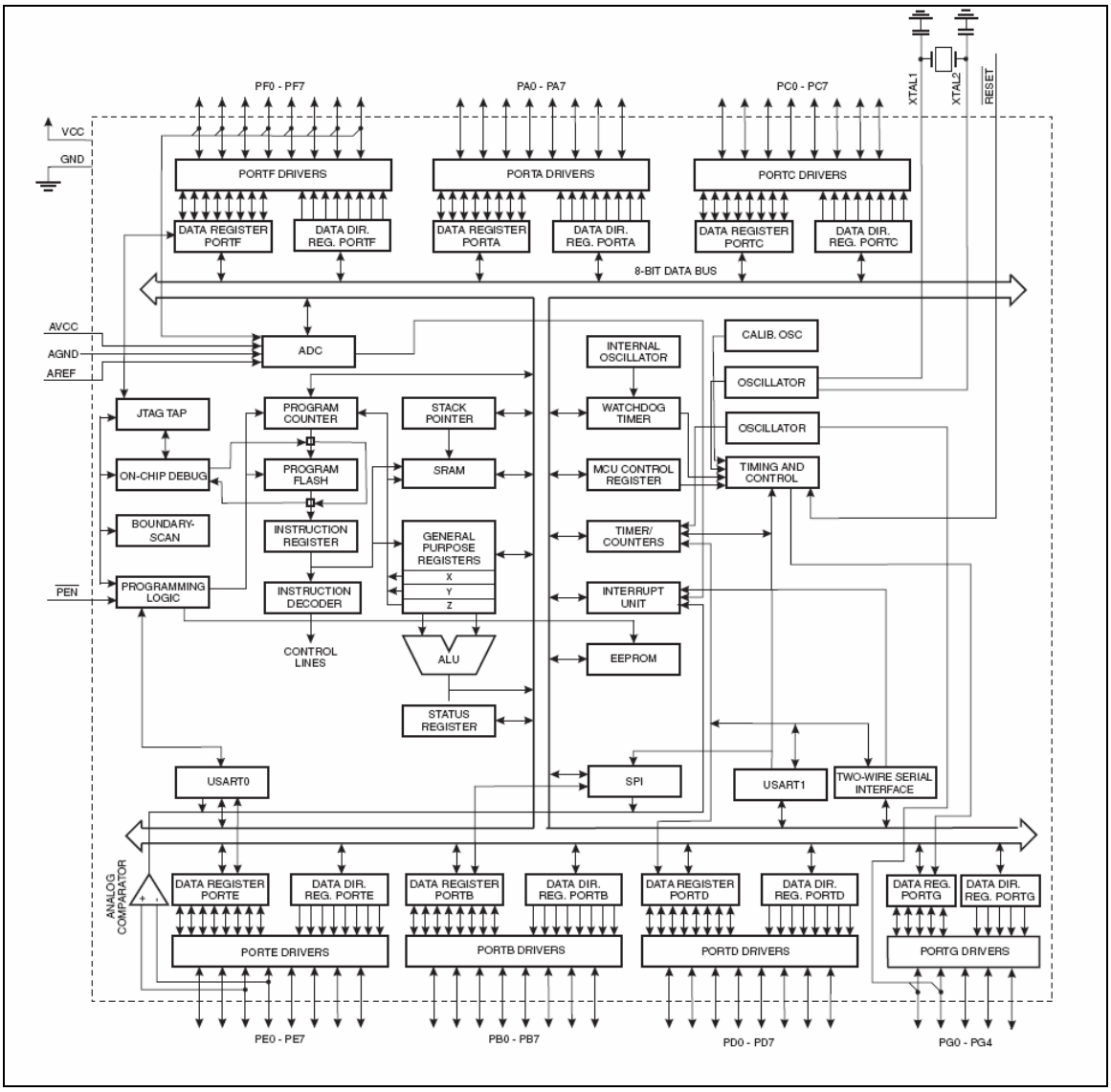

FIGURE 2: Architecture of Atmega 128L [1, p3]

The ATmega 128L provides the following features: 128K bytes of in-system programmable flash with read-while-write capabilities, 4K bytes of EEPROM, 4K bytes of SRAM, 53 general purpose I/O lines, 32 general purpose working registers, real time counter (RTC), four flexible timer/counters with compare modes and PWM, 2 USARTs, a byte oriented two-wire serial interface, a 8-channel, 10-bit ADC with optional differential input stage with programmable gain, programmable watchdog timer with

internal oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the on-chip debug system and programming, and six software selectable power saving modes.

During the Idle mode the CPU is disabled while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The power-down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset. In power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC noise reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC to minimize switching noise during ADC conversions. In standby mode, the crystal/resonator oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In extended standby mode, both the main oscillator and the asynchronous timer continue to run [1].

The on-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an on-chip boot program running on the AVR core. The boot program can use any interface to download the application program in the application flash memory. Software in the boot flash section will continue to run while the application flash section is updated, providing true read-while-write operation. By combining an 8-bit RISC CPU with in-system self-programmable flash on a monolithic chip, the Atmel ATmega 128L is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications. The ATmega 128L AVR is supported with a full

suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits [1].

3.1.3 Overview of Coulomb Counter

The DS2740 – high precision coulomb counter with 65µA/1µA current consumption in active/sleep modes respectively was initially designed for battery monitoring, but can be used to monitor consumption of any device. In the active mode of operation, the DS2740 continually measures the current flow into and out of the device under observation by measuring the voltage drop across a low-value current-sense resistor, $R_{SNS.}$ The voltage-sense range is ±51.2mV. To extend the input range for pulse-type load currents, the voltage signal can be filtered by adding a capacitor between the IS1 and IS2 pins as shown in Figure 3. The external capacitor and two internal 10kΩ resistors form a low pass filter at the input of the ADC. The input converts peak signal amplitudes up to 75mV as long as the continuous or average signal level (post filter) does not exceed ±51.2mV over the conversion cycle period. The ADC samples the input differentially and updates the current register (CR) at the completion of each conversion cycle.

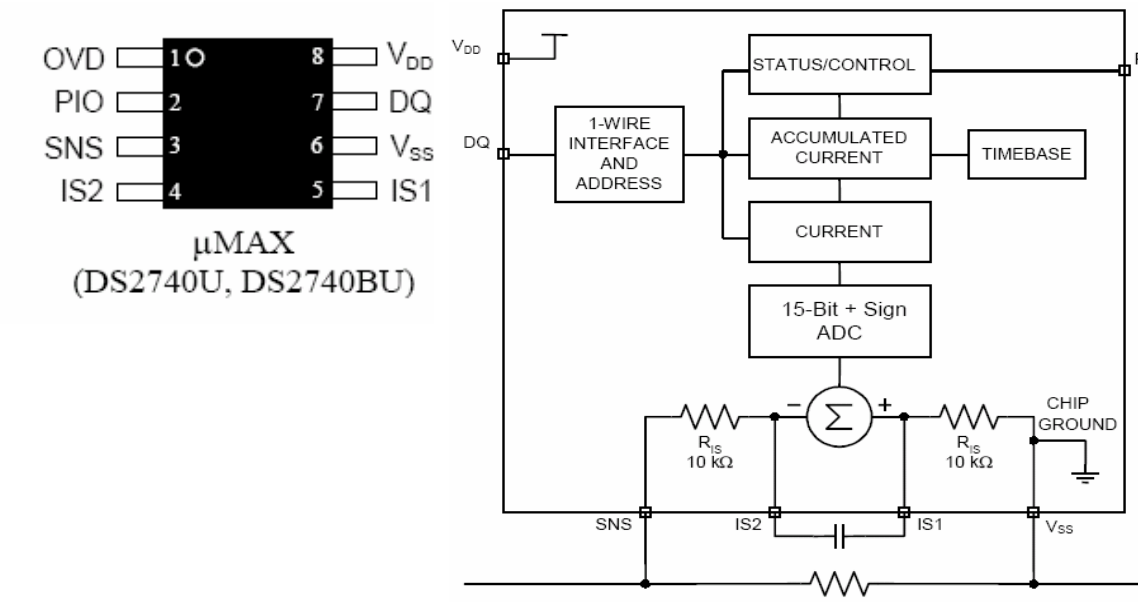

FIGURE 3: Pin Description and Block Diagram of DS2740 [4, p1, p4]

There are two versions of DS2740 available: 15- and 13- bit A/Ds. With identical analog circuits the 15-bit version has a conversion period 4 times longer then the 13-bit version (3.2s versus 0.875s), and hence, 4 times better resolution and dynamic range. For 15-bit (DS2740) and 13-bit (DS2740B) devices, the resolution (LSB) is 1.56µV and 6.25µV respectively. One possible drawback of higher sensitivity is prolonged conversion that may be critical in real-time applications. The range of measuring current depends on a sense resistor R_{SNS} and can be adjusted widely. The value of R_{SNS} is calculated based on maximum consumption I_{max} and is equal to $\boldsymbol{R_{SNS}=51.2mV/I_{max}}$. Current resolution is $\boldsymbol{6.25\mu V/R_{SNS}}$ and $\boldsymbol{1.56\mu V/R_{SNS}}$ for 13-bit and 15-bit versions, respectively. Thus for the 13-bit device using R_{SNS}=0.02Ω, the current resolution is 312µA LSB and dynamic range ±2.56A. For R_{SNS}=0.1Ω, the current resolution and dynamic range are 62.4µA and ±512 mA respectively. The current measurement offset range is –3 LSBs to +5 LSBs according to datasheet specification. The positive average

offset error +1 LSB caused by sharing one sense line with device ground through VSS and can be reduced by an average of 2 LSBs (1.9mAh per day with a 20mΩ sense) by eliminating internal resistors of RC filter and connecting IS1 and IS2 directly to the sense resistor. The loss of the filter will have no impact in most applications. In pulse-load cases with current spikes larger than the dynamic range of the A/D external filter can be used. Every 1024th conversion (15 minutes in the DS2740B), the ADC measures its input offset to facilitate offset correction. During the offset correction conversion, the ADC does not measure the IS1 to IS2 signal. To reduce the error, the current measurement just prior to the offset conversion is displayed in the Current Register and is substituted for the dropped current measurement in the current accumulation process. Due to the nature of DS2740's current sensing, special precautions need to be taken in the systems with multiple connections between devices. Electrical connections may create go-round current leaks and may compromise measurement. In order to prevent unwanted current flows bypassing R_{SNS}, all connections to CC2420 were made through Coulomb counter [4].

CURRENT ACCUMULATOR

Current measurements are internally summed at the completion of each conversion period with the results displayed in the Accumulator Current Register (ACR). The ACR has a range of ±204.8mVh with Current Accumulation Register resolution 6.25µVh (Both DS2740 and DS2740B). For R_{SNS}=0.02mΩ, the ACR resolution is 312.5µAh and the range is ±10.24Ah. Read and write access is allowed to the ACR. A write forces the ADC to measure its offset and update the offset correction factor. The current

measurement and accumulation begin with the second conversion following a write to the ACR.

MEMORY

The DS2740 has memory space as registers for instrumentation, status, and control. When the MSB of a two-byte register is read, both the MSB and LSB are latched and held for the duration of the read data command to prevent updates during the read and ensure synchronization between the two register bytes. The register memory map is shown in Table 2.

MEMORY MAP

ADDRESS (HEX)	DESCRIPTION	READ/WRITE
00	Reserved	--
O1	Status Register	R
02 to 07	Reserved	--
08	Special Feature Register	R/W
09 to 0D	Reserved	--
0E	Current Register MSB	R
OF	Current Register LSB	R
10	Accumulated Current Register MSB	R/W
11	Accumulated Current Register LSB	R/W
12 to FF	Reserved	--

TABLE 2 : Memory Map of DS2740

SPECIAL BITS

- SMOD: SLEEP Mode Enable. Status Register bit. A value of 1 allows the DS2740 to enter sleep mode when DQ is low for 2s. The power-up default of SMOD = 0.
- RNAOP: Read Net Address Opcode. Status Register bit. A value of 0 in this bit sets the opcode for the read net address command to 33h, while a 1 sets the opcode to 39h. Addressing different opcodes help save time in multi-slave systems.
- PIO: Pin Sense and Control. Special Features Register bit. This bit is read and write enabled. Writing a 0 to the PIO bit enables the PIO open-drain output driver, forcing the PIO pin low. Writing a 1 to the PIO bit disables the output driver, allowing the PIO pin to be pulled high or used as an input. Reading the PIO bit returns the logic level forced on the PIO pin [5].

3.2 Description of the Board

The CC2420 is a single-chip IEEE 802.15.4 compliant and ZigBee ready RF transceiver. It provides a highly integrated, flexible low-cost, low power solution for applications using the world wide unlicensed 2.4 GHz frequency band. The Embedded Evaluation Board is a prototyping platform for application code. This board contains a CC2420 with necessary support components, an Atmel ATmega 128L AVR microcontroller, a SMA connector, switches and LED's are also provided for better testability. The board is also furnished with connectors where all of the internal signals on the PCB are available. The CC2420 RF section includes all the necessary components for correct operation. The CC2420 is connected to a 16 MHz crystal. RF test and

measurement equipment can be connected to the SMA on the PCB. The power supply section contains two voltage regulators: a 3.3 V regulator for use by the microcontroller and another for use by the I/O pins of the CC2420. The internal regulator of CC2420 is used to generate the 1.8 voltage supply applied for powering of the CC2420 core. A diode prevents permanent damage if wrong polarity is applied to the board. The MAX3243 is used as the serial port driver and receiver that consists of three line drivers, five line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). The device provides the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches that needed for the typical serial port. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active non-inverting output which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/μs driver output slew rate [14]. There is also a JTAG interface for flashing the microcontrollers and on-chip debug. The in-system programming connector on the board allows programming and reprogramming of the microcontroller. Using a simple 3-wire SPI interface, the in-system programmer communicates serially with the ATmega 128L, reprogramming all nonvolatile memories on the chip. Figure 4 shows the architecture of the board.

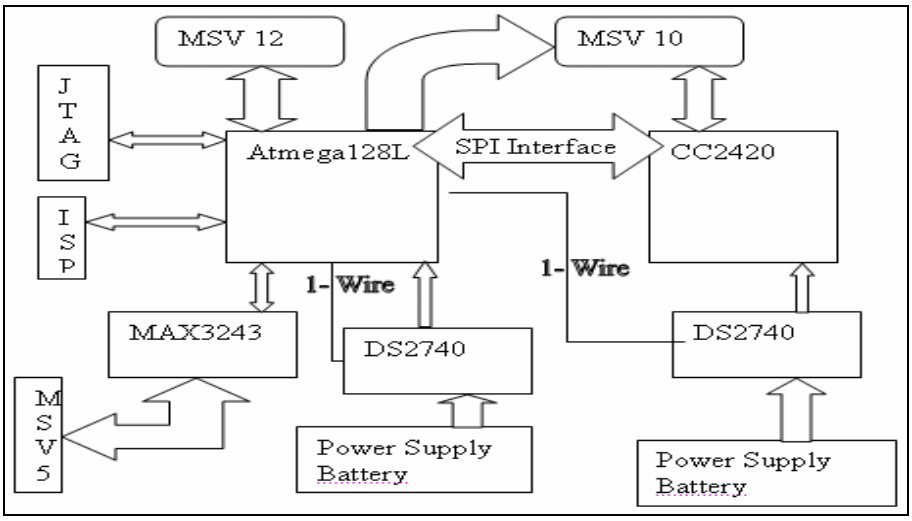

FIGURE 4: Architecture of the Embedded Wireless Board

CHAPTER 4: INTERFACING HARDWARE

4.1 Interfacing ATMEGA 128L and CHIPCON RF Section

The ATmega 128L is interfaced with the CC2420 using the SPI interface. The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the ATmega 128L and CC2420 or between several AVR devices. The ATmega 128L SPI includes a full-duplex and a three-wire synchronous data transfer and can operate as a master or a slave. The data transfer in the SPI can be configured to occur either with LSB first or MSB first. Seven programmable bit rates allow the interface to operate at the user specified rate. An end of transmission interrupt flag and write collision flag protection is provided for easier and reliable code development. It can be set at two different operating modes, namely wake-up from idle mode and double speed (CK/2) master SPI mode.

In this interfacing the ATmega 128L is configured as the master and the CC2420 as the slave. The SPI Interface uses the four pins described as follows. The SPI master initiates the communication cycle when pulling the slave select (SS) pin of the CC2420 low. The master and slave prepare the data to be sent in their respective shift registers, and the master generates the required clock pulses on the SCK line to interchange data.

Data is always shifted from master to slave on the Master Out – Slave In (MOSI) line, and from slave to master on the Master In – Slave Out MISO line. After each data packet, the master will synchronize the slave by pulling high the Slave Select SS line.

PIN	Direction, Master SPI	Direction, Slave SPI
MOSI	User Defined	Input
MISO	Input	User Defined
SCK	User Defined	Input
SS	User Defined	Input

TABLE 3: SPI Pin Overrides

The direction of the SPI pin configuration is listed in Table 3. When the SPI is configured as a master, the user can determine the direction of the SS pin. If SS is configured as an output, the pin is a general output pin that does not affect the SPI system. Typically, the pin will be driving the SS pin of the SPI slave. If SS is configured as an input, it must be held high to ensure master SPI operation. If the SS pin is driven low by any peripheral and the SPI is configured as a master with the SS pin defined as an input, the SPI system interprets this as another master selecting the SPI as a slave and starting to send data to it. When the SPI is configured as a slave, the Slave Select (SS) pin is always input. When SS is held low, the SPI is activated, and MISO becomes an output if configured so by the user. All other pins are inputs. When SS is driven high, all pins are inputs, and the SPI is passive, which means that it will not receive incoming data. The SPI logic will be reset once the SS pin is driven high. The SS pin is useful for packet/byte synchronization to keep the slave bit counter synchronous with the master clock generator. When the SS pin is driven high, the SPI slave will immediately reset the send and receive logic, and drop any partially received data in the shift register [8].

The ATmega 128L microcontroller uses 4 I/O pins for the SPI Configuration Interface (SI, SO, SCLK and CSn). SO should be connected to an input at the microcontroller. SI, SCLK and CSn must be microcontroller outputs. The microcontroller pins connected to SI, SO and SCLK can be shared with other SPI-interface devices. SO is a high-impedance output as long as CSn is not activated. CSn should have an external pull-up resistor or be set to a high level when the voltage regulator is turned off in order to prevent the input from floating. SI and SCLK should be set to a defined level to prevent the inputs from floating. The ATmega 128L can program CC2420 into different modes, read and write buffered data, and read back status information via the 4-wire SPI-bus configuration interface (SI, SO, SCLK and CSn). The microcontroller is also interfaced to the receive and transmit FIFOs using the FIFO and FIFOP status pins. It is also interfaced to the CCA pin for clear channel assessment and SFD for timing information. The interfacing between the ATmega 128L and CC2420 is shown in the Figure 5.

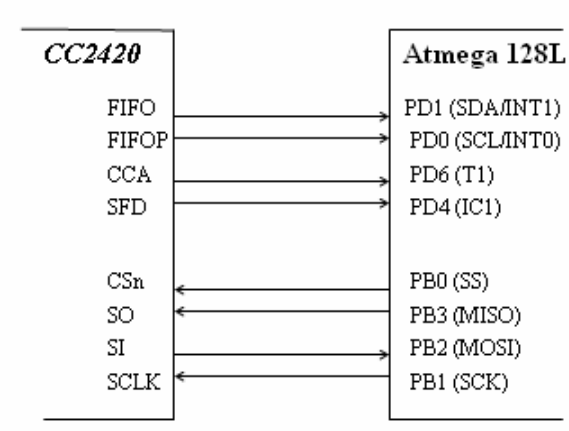

FIGURE 5: SPI Interface between ATmega 128L and CC2420

The RF I/O pins on CHIPCON RF_P and RF_N are connected to the SMA connector through the TXRX_Switch for proper RF matching. RF data and test measurements can

be done through the SMA connector. The SPI interface pins and some of the Digital I/O pins of the CHIPCON are routed to a header and can be used for debugging in case of any errors.

4.2 Interfacing ATMEGA 128L, CHIPCON and Coulomb Counter

The Dallas Semiconductor 1-Wire bus is a simple signaling scheme that performs two-way communications between a single master and peripheral devices over a single connection. The 1 wire bus system has a single bus master and one or more slaves. A multidrop bus is a 1-Wire bus with multiple slaves. A single-drop bus has only one slave device. In all instances, the DS2740 is a slave device. The bus master is typically a microprocessor in the host system. In this board the bus master is the microcontroller ATmega 128L. The hardware configuration considerations for the 1 wire bus are as follows:

- 1-Wire bus has a single line so it is important that each device on the bus must be able to drive it at the appropriate time. To ensure this, each device attached to the 1-wire bus must connect to the bus with open-drain or tri-state output drivers. If a bidirectional pin is not available on the bus master, separate output and input pins can be connected together.
- The 1-Wire timing protocol has specific timing constraints that must be followed in order to achieve successful communication. The DS2740 can operate in two communication speed modes, standard and overdrive. The speed mode is determined by the input logic level on the OVD pin.

- The 1-Wire bus must have a pull-up resistor at the bus-master end of the bus. For short line lengths, the value of this resistor should be approximately 5kΩ. The idle state for the 1-Wire bus is high.

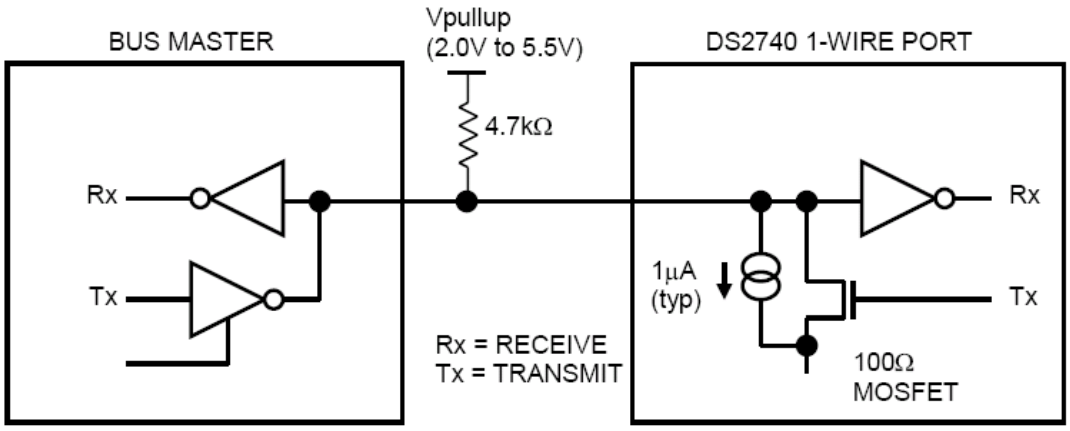

FIGURE 6: 1- Wire Bus Interface Circuitry [4, p10]

Figure 6 shows the requirements for the 1 – Wire bus interface circuitry. Figure 10 and Figure 11 illustrate the interfacing between the ATmega 128L, CC2420 and the DS2740. The 150 ohms resistors from 3.3AV and 3.3CV to VDD of the respective DS2740 are for ESD immunity. The resistor helps limit current spikes into the part, and protect against over-voltage conditions. The other passive component on the VDD line is the 0.1μF capacitor. This capacitor helps to filter voltage spikes and maintains the voltage within the specified range. The ATmega 128L data pin is an open drain driver similar to the Data I/O (DQ) pin of the DS2740. The DATA and DQ pins are directly connected together, and a 4.7kΩ pull-up resistor is used to pull the data line to logic high. The DS2740 1-Wire bus speed control (OVD) pin is connected to VSS indicating standard 1-Wire timing protocol. For overdrive timing, the OVD pin should be tied to the VDD pin of the part. To monitor the voltage across the sense resistor (RSNS), the SNS pin is connected to the host side of RSNS and VSS is connected to the cell side. The current-

sense input pins (IS1 and IS2) are connected to either end of a 0.1μF capacitor. This capacitor and the internal resistors provide a low pass filter for current spikes. The device ground, VSS, must always be connected to the negative terminal of the voltage regulator. The last pin, PIO, is an open-drain, general-purpose input/output driver. PIO is not necessary for proper device functionality, but can be used for driving an LED or vibrating motor [5].

4.3 Interfacing ATMEGA 128L with Other Components

The 802.15.4 Evaluation Board has a JTAG connector that can be used to program flash, EEPROM, fuses, and lock bits and provides on-chip debug support. It provides debugger access to all internal peripheral units, internal and external RAM, internal register file, program counter, EEPROM and flash memories. The JTAG interface is accessed through four of the AVR's pins. In JTAG terminology, these pins constitute the Test Access Port — TAP. These pins are:

- TMS: Test Mode Select. This pin is used for navigating through the TAP-controller state machine.
- TCK: Test Clock. JTAG operation is synchronous to TCK.
- TDI: Test Data In. Serial input data to be shifted in to the instruction register or data register.
- TDO: Test Data Out. Serial output data from instruction register or data register [9].

The 802.15.4 Evaluation Board also has a connector for in system programming (ISP). To program any AVR microcontroller in any target system, a simple 6-wire

interface is used to connect the programmer to the target PCB. Figure 7 shows the connections needed.

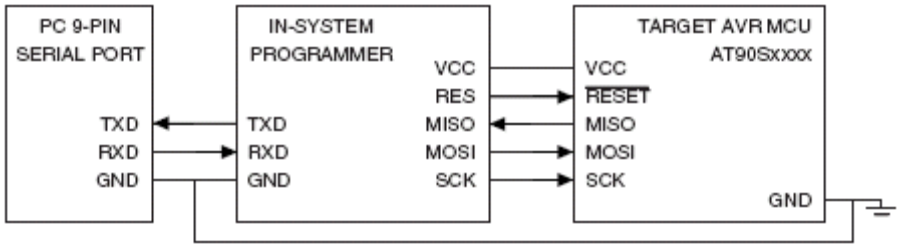

FIGURE 7: 6-wire Connection between Programmer and Target System [16]

The ISP Programmer shown in Figure 7 is a part of the ATmega 128L, so just the serial port interface is required with the ATmega 128L. The ISP connector uses the SPI interface to program the target microcontroller. The Serial Peripheral Interface (SPI) consists of three wires: Serial Clock (SCK), Master In – Slave Out (MISO) and Master Out – Slave In (MOSI). When programming the AVR, the in-system programmer always operates as the master, and the target system always operate as the slave. The In-System programmer (master) provides the clock for the communication on the SCK line. Each pulse on the SCK line transfers one bit from the programmer (master) to the target (slave) on the Master Out – Slave In (MOSI) line. Simultaneously, each pulse on the SCK line transfers one bit from the target (slave) to the programmer (master) on the Master In – Slave Out (MISO) line. The In-System programmer and target system need to operate with the same reference voltage. This is done by connecting ground of the target to ground of the programmer. The target AVR microcontroller will enter serial programming mode only when its reset line is active (low). When erasing the chip, the reset line has to be toggled to end the erase cycle. The in-system programmer draws power from the target microcontroller [16].

Three LED's are connected to port pins of the microcontroller and can be used for debugging purposes. Similarly the push button switch can be used as an input for debugging purposes. Another switch is for resetting the microcontroller and is connected to the RESET pin of the ATmega 128L.

The 802.15.4 board also contains a serial connector for RS-232 serial communications. The MAX3243 RS-232 Line Driver/Receiver is used for level shifting of the voltages between the PC and the microcontroller. The RS232_TD and RS232_RTS pins of the serial connector are connected to the receiver input R1IN and R2IN. The other three receiver inputs are grounded. The driver outputs T1OUT and T2OUT are connected to the RS232_RD and RS232_CTS pins of the serial connector. The TXD1 and CTS pins of the microcontroller are connected to the driver inputs T1IN and T2IN of the MAX3243. The RX1 an RTS of the microcontroller are connected to the receiver output pins R1OUT and R2OUT. The four external capacitors allow operation from the 3.3V supply and are there for ESD immunity. Flexible control options for power management are available when the serial port is inactive. The auto-power down feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 μA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-power down condition to occur.

The extra I/O port pins of the microcontroller that are not being used are routed to headers. These pins can be used in future for interfacing sensors or for debugging purposes.

CHAPTER 5: DESIGNING SCHEMATICS

5.1 Overview of OrCAD

OrCAD is a software tool for schematic design. It can be used to design analog circuits, revise digital schematic diagram for an existing PCB or complete a hierarchical block design. Apart from designing, it also provides various built-in features for design verification and manufacturing processing. OrCAD capture provides a component information system that allows one to identify, utilize and design with preferred parts. In the following subsection, a detailed description of the features provided by OrCAD capture and OrCAD layout are discussed [12].

5.2 Features of OrCAD Capture CIS

Capture stores all of the design's schematics, schematic pages, and parts in a single file. This makes it easy to handle our designs. Capture displays the design in a project manager. The project manager provides an organized view into the contents of the design files. A design is a collection of schematic folders. It contains hierarchy and back annotation information, as well as a design cache. A capture design can contain one or more schematic folders and each schematic folder can contain one or more schematic pages. A schematic folder is simply a collection of schematic pages that are logically connected by off-page connectors or hierarchical ports and pins. The design cache serves as an archive of each unique parts and symbols used in the design. Off-page connectors or separate schematic pages within a schematic folder are electrically connected if they

have the same name. Similarly, wire segments and off-page connectors on the same schematic page are electrically connected if they have the same name.

Capture CIS also has a feature called the Session Frame, shown in Figure 8. The session frame contains a log of activities that occur during the Capture session. If you update part references or properties, create a netlist, or check design rules, information is recorded in the session log, which appears in the session frame. Capture's pull down menus and shortcut keys make editing a schematic page an easy task. The right mouse button provides fast access to all the editing functions for the selected objects.

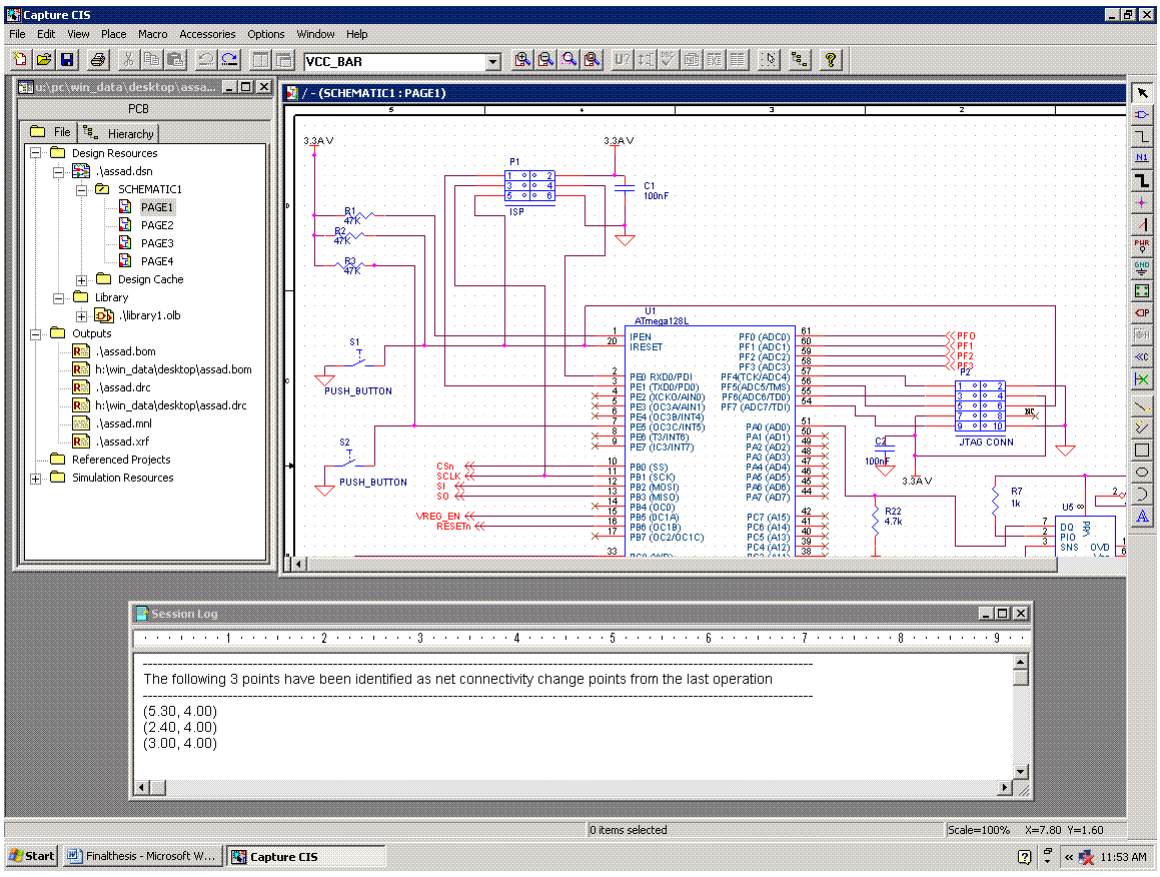

FIGURE 8: Capture Design window with Session log, Tool palette and Project Manager

Capture makes it easy to place the parts for your design. After placing the parts and electrically connecting them all the electrical information is stored in the design, making it easy to progress from placing parts to creating a netlist. When you place a part on a schematic page, the part can be placed without a reference designator assigned to it, or it can have one automatically assigned.

5.3 Features of OrCAD Layout

OrCAD Layout is a powerful circuit board layout tool and has all the automated features to quickly complete a board design. The netlist created by Capture CIS is used by Layout to create the board. Changes made in the schematics are automatically updated in the board Layout by Auto ECO, which is a feature provided by OrCAD. Auto ECO is an Automatic Engineering Change Order Process that keeps track of the changes made in the netlist and part references in the schematic design. OrCAD Layout also has the auto placement utility that allows one to place components individually, in groups, in clusters or the entire board. Manual as well as auto routing is possible in OrCAD Layout. In auto routing Layout's auto router uses sweep, shove and interactive routing technology to provide maximum auto routing power and flexibility. Other important features like intelligent copper pour, design reuse provides simplicity in design process while routing density display enables efficient routing. For post processing, Layout produces hardcopy for printers and plotters, and also produces Gerber files, DXF files and a wide variety of report files [13].

5.4 Making New Libraries and Parts

With capture we do not have to keep track of multiple libraries. All the information Capture needs about every part in the design is kept in the design itself. Designs in

Capture are self-contained and portable. The project manager displays all the parts in the library if you open and expand it. A library can contain parts, packages, symbols and schematic folders. In a library, they are all treated as parts. It is possible to move parts from one library to another by just dragging and dropping it. You can also copy a schematic folder to a library.

Most of the parts used in the evaluation board were unavailable in the Capture Libraries so I had to make custom parts for some of the chips. To store all of these parts a new library was created, library1.obk. It is very straightforward to create libraries in Capture. In the file menu, select "new library" and a new library gets added to the design. The parts mentioned above were added to this library. To create new parts in Capture:

- Select the library in the project manager and click "New Part" in the Design menu
- In the New Part Properties Dialog box assign a part name, a part reference prefix, and a name for its assigned PCB footprint
- An empty part outline appears in the part editor. To draw the part, use the place menu commands or the tool palette drawing tools
- To add pins from the place menu click pin
- Specify the pin name and number, and whether the pin represents one signal or a bus
- Pin shape and type determine the pin's appearance and electrical characteristics
- Now place the pin. If you place more than one pin, Capture automatically increments the pin numbers
- After placing all the pins from the file menu, click Save to save the finished part

Using the steps above, new parts CC2420, ATmega 128L, MAX3243, DS2740 and MIC5209-3.3BS were designed and are shown in Figure 9.

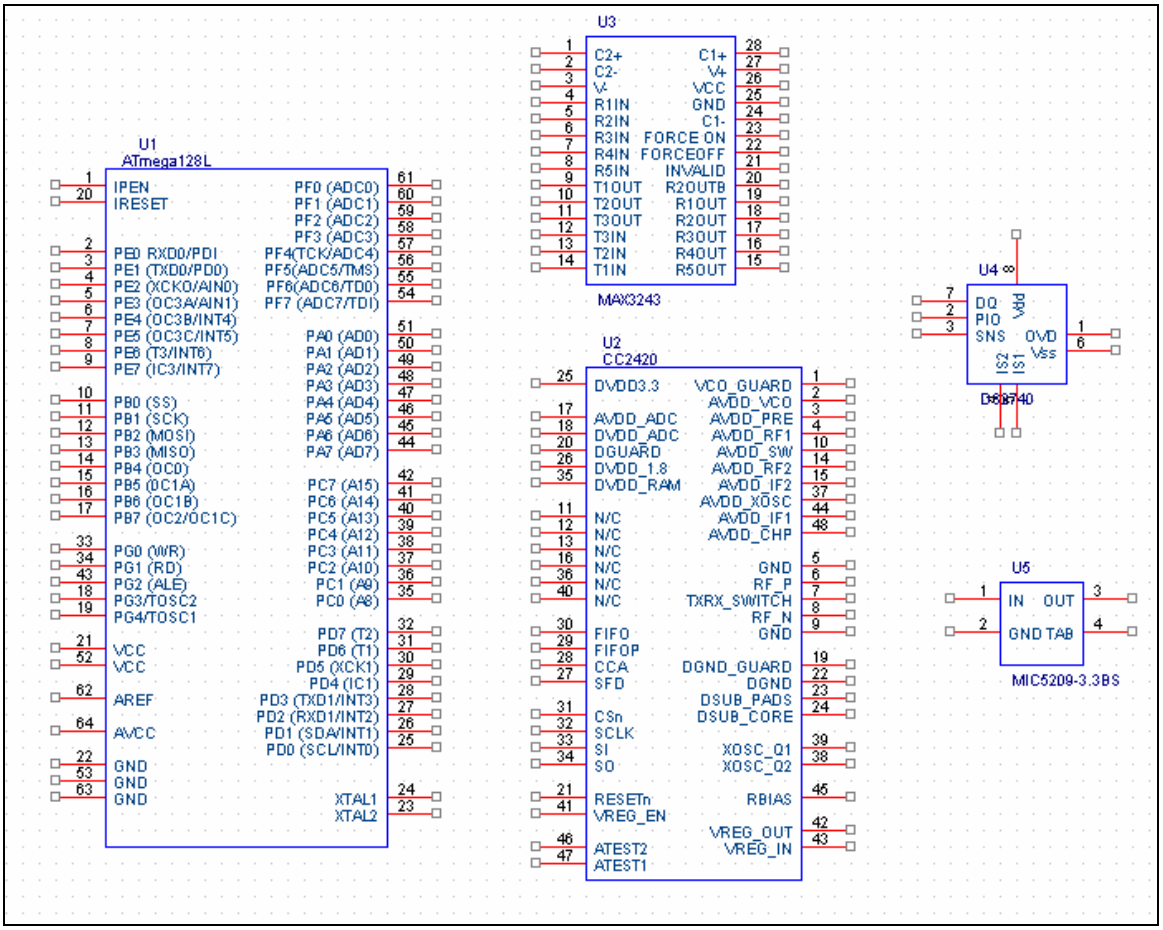

FIGURE 9: ATmega 128L, CC2420, MAX3243, DS2740 and MIC5209-3.3BS

These parts shown in Figure 9 and the parts that were already in the capture libraries required for the design were placed on the schematics. The electrical connections were made between the parts using the tool palette and the final schematics were made.

5.5 Schematics

Figure 10 shows the page 1 of the schematic design of the wireless embedded board. It illustrates the one-wire interface between the ATmega 128L microcontroller and

MAXIM DS2740 coulomb counter. It also shows the one-wire being pulled high at the microcontroller side with a 4.7 kΩ resistor. An external crystal oscillator is connected between XTAL1 and XTAL2 of ATmega 128L. The schematic also shows the JTAG and ISP connectors interfaced to the respective ports of the microcontroller. The reset switch S1, switch S2 and the three on board LED's are also illustrated. The signals coming out of the ATmega128L are marked with arrows pointing outwards. This signifies the connection to other peripheral components in the schematic design on a different page.

Figure 11 shows page 2 of the schematic design. It shows the power supply to the CC2420 through the coulomb counter. The CON5 represents the SMA connector connection with the necessary active and passive components. MSV4 is a 4 pin header for mounting an external crystal oscillator for the RF section. The signals marked with arrows are off page connectors and are connected to the microcontroller.

Figure 12 shows the page 3 of the schematic design. It has 2 voltage regulators MIC5209-3.3 and MIC5209-3.3 for the microcontroller section and the RF section respectively. It also shows the serial port header MSV5. The header with unused port pins MSV5x2 and the header with internal signals MSV12 are also illustrated.

Figure 13 shows page 4 of the schematic design shows the MAX3243 RS 232 line driver/receiver. It serves as the interface between the ATmega 128L and the serial port. It is connected to the microcontroller and the serial port through off page connectors.

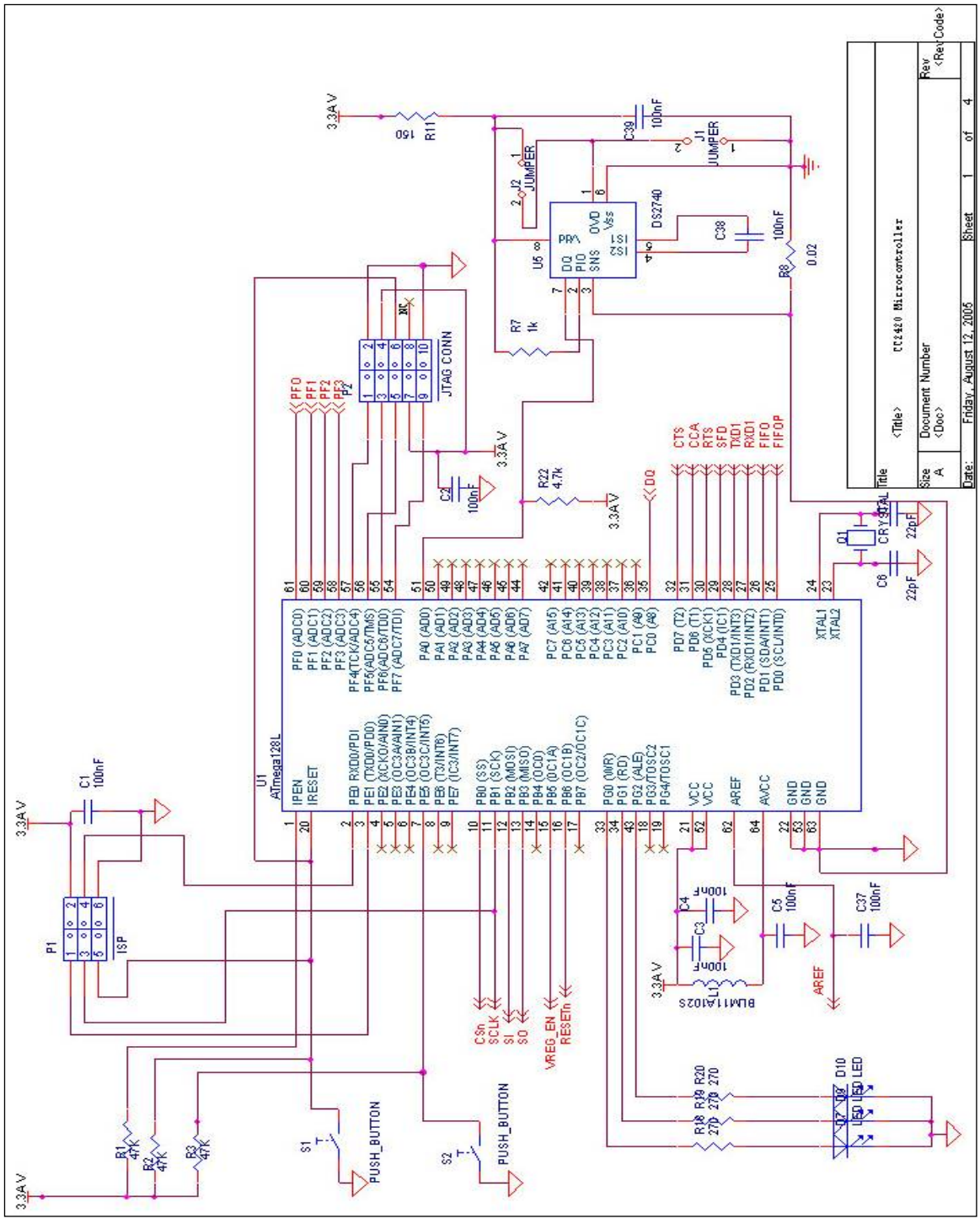

FIGURE 10: Microcontroller ATmega 128L interfaced with Coulomb counter DS2740

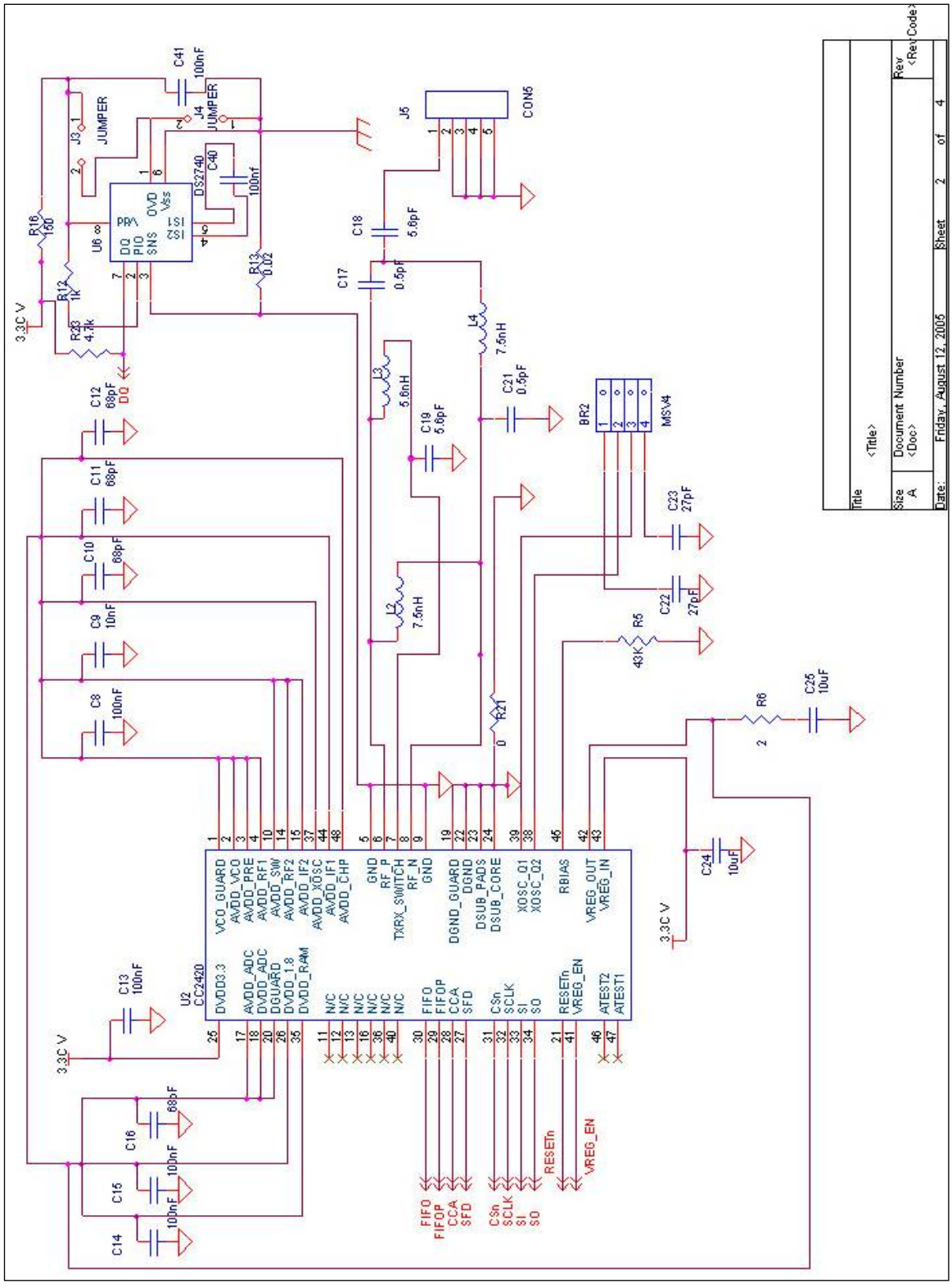

FIGURE 11: RF Transceiver CC2420 interfaced with Coulomb Counter DS2740

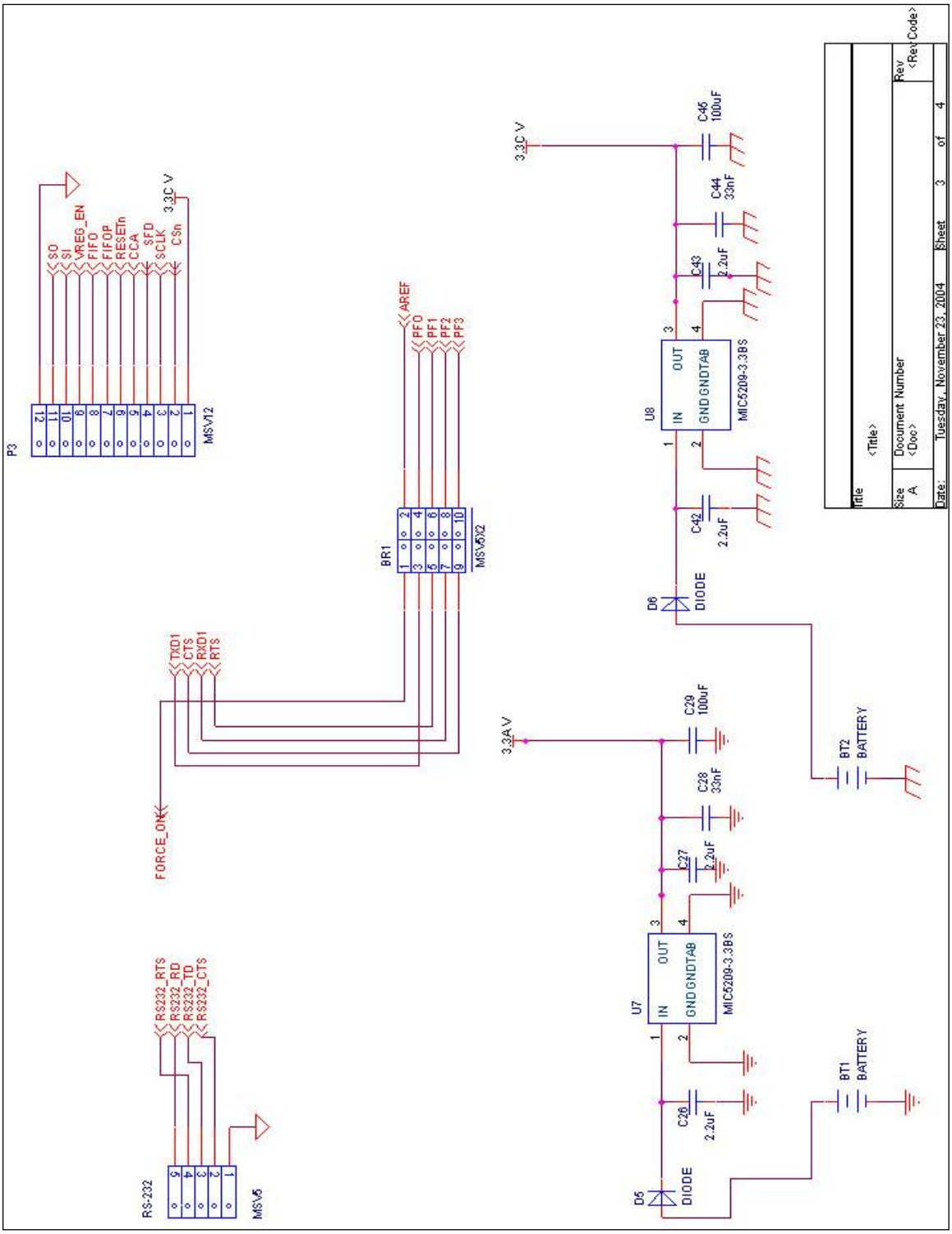

FIGURE 12: Power Supply for ATmega 128L and CC2420 with some headers

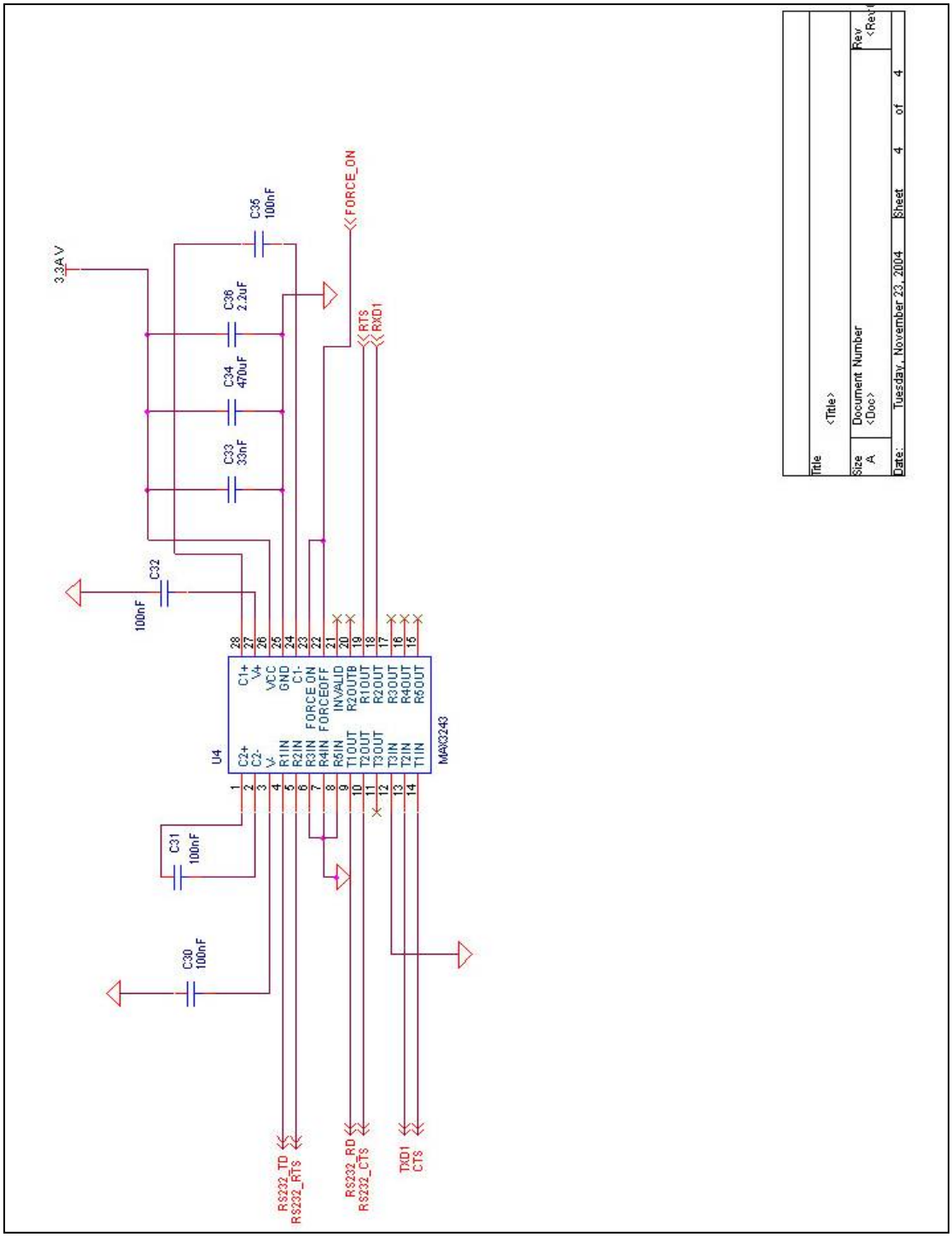

FIGURE 13: MAX3243 RS-232 line Driver/Receiver

5.6 Processing the Design

Once the design was drawn, parts and pages were connected. The next steps were to update the part references, verify the designs integrity and create a netlist. Capture provides all the tools needed to process the design in one menu that is shown in Figure 14.

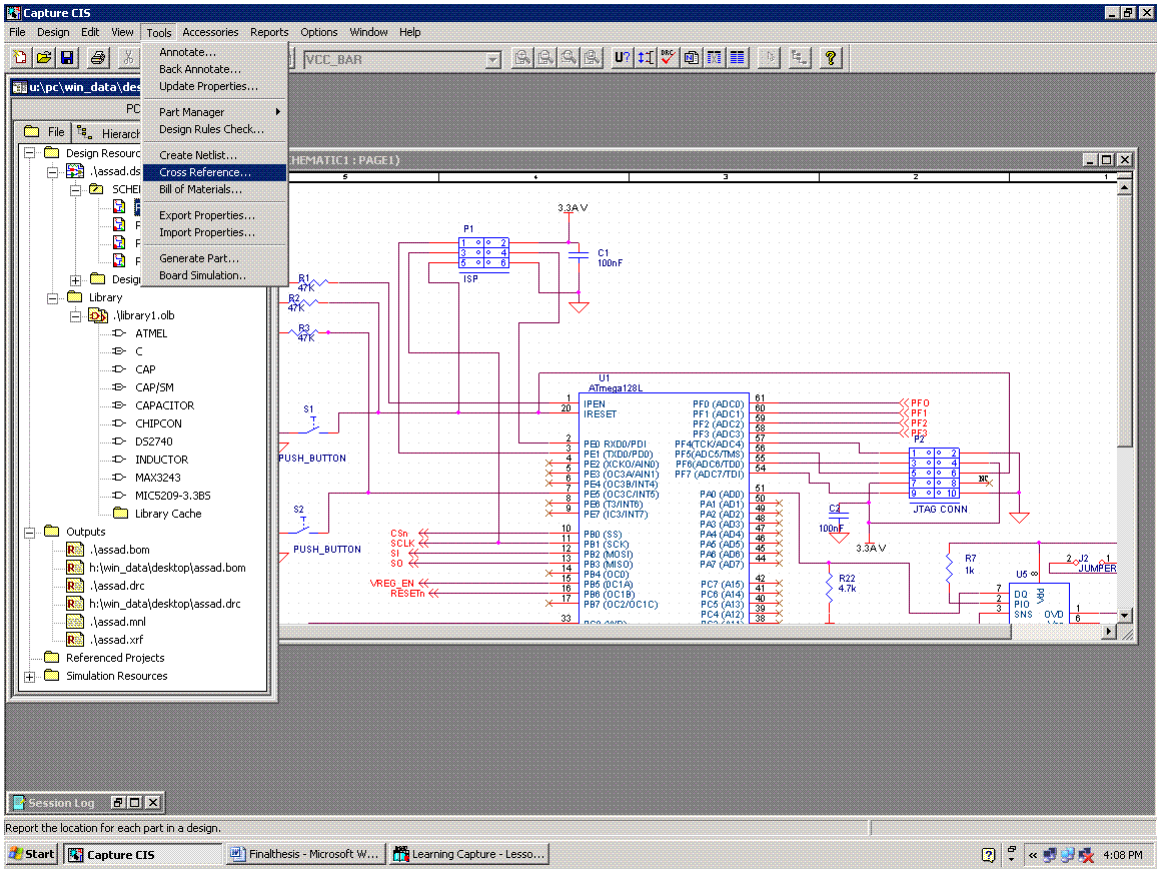

FIGURE 14: Tools menu showing the Post Processing Commands

By choosing the Annotate command in the tools selection all the part references were assigned. All the parts that were not manually assigned references earlier were assigned automatically. Annotate gives us the option of updating references for the entire design or just a schematic page. One can also choose the type of reference update wanted. To

locate any DRC errors and check the integrity of the design, the Design Rules Check command from the Tools menu was used. It allows specifying the scope and action of the DRC. If “create DRC markers for warnings” is selected, Capture places DRC error markers on all affected schematic pages. After removing all the DRC errors, the netlist was created to produce a circuit board layout of the PCB design. To create the netlist, the design was selected and the Create Netlist command from the Tools menu was used.

CHAPTER 6: PCB DESIGNING USING LAYOUT

6.1 Setting up the Board Using OrCAD Layout

The following steps were taken for setting up the board

- The netlist and the target directory for the design was specified
- The units of measurement was selected
- The board outline was defined
- The layer stack was defined
- System grid was set
- The footprints of the components used in the design was specified
- The manufacturing technology was specified
- Spacing rules was specified
- Padstacks and Vias were defined

It was very easy to do all these things using Layout. From the File menu "New" was clicked. The AutoECO dialog box appeared. There the technology template and the netlist to be used for the PCB design were specified. A technology template contains everything that can be included in the design, except the netlist. It defines the board layers, default grids, spacing track widths and padstacks. It also includes Gerber standards, design rules, drawing formats, dimensions, pre-placed components and tooling holes. The technology template used for the design was Surface Mount Technology since most of the components in the design are Surface Mount devices. The netlist specifies the connectivity information and component types for the design. Then the location of the

new layout board file was specified. The AutoECO option was used to configure the board. The AutoECO prompts to link the components to the footprints. If the footprint doesn't exist one can modify the existing footprints to one's requirements and use them. The units of measurement were chosen to be mils. This was done in the System settings in the Options menu. The technology template assigns a default board outline which had to be changed. This was done using the Obstacle Tool toolbar button. In the Edit Obstacle dialog box the obstacle layer was selected as Global and the obstacle type as board outline. The length of the board is 2.3 inches and the breadth is 3 inches. Then the board outline was made in the design window. In the View spreadsheet tool bar button the layers spreadsheet was selected to modify the number of layers used in the design. In the 802.15.4 board there are only two layers, Top and Bottom, and they both are used for routing. Separate power and ground layers were not used to reduce the cost of the board. Using the Route spacing option in the View spreadsheet toolbar button the global spacing rules for the pads, tracks and vias in the design was defined. After setting up the board the components were placed on the board using a variety of powerful placement commands offered. The components were placed in such a manner that routing becomes very easy after the placement.

6.2 Making New Padstacks, Footprints and Libraries

Footprints for most of the chips in the design were not available in the Layout libraries so new footprints were created. The padstacks used for these footprints were mostly rectangular in shape. These were also not present in the padstacks spreadsheet so new padstacks were created. Creating a new padstack is simple using Layout. To create a new padstack

1. Choose the spreadsheet toolbar button, and then choose Padstacks. The Padstacks spreadsheet appears.
2. Right click the mouse on the spreadsheet and select New from the pop-up menu. A new padstack is added at the bottom of the spreadsheet.
3. Select the new padstack and choose properties from the pop-up menu.
4. Type a new name for the padstack in the padstack text box. Edit other properties such as the size and shape as desired and then click OK.
5. Make specific layer definitions for the padstack for the drill and plane layers

The padstacks created for the 802.15.4 were for footprints for Surface Mount Technology devices. These padstacks were therefore not present on the bottom layer they were just on the top layer.

To make the footprints for the components, the Pad Array Generator was used. The new footprints were created by following the steps:

1. Open the Library manager and select the create new footprint option
2. From the Create New Footprint dialog box, select the Use Pad Array Generator option. The Pad Array Generator dialog box and Array Preview window appear (see Figure 15).

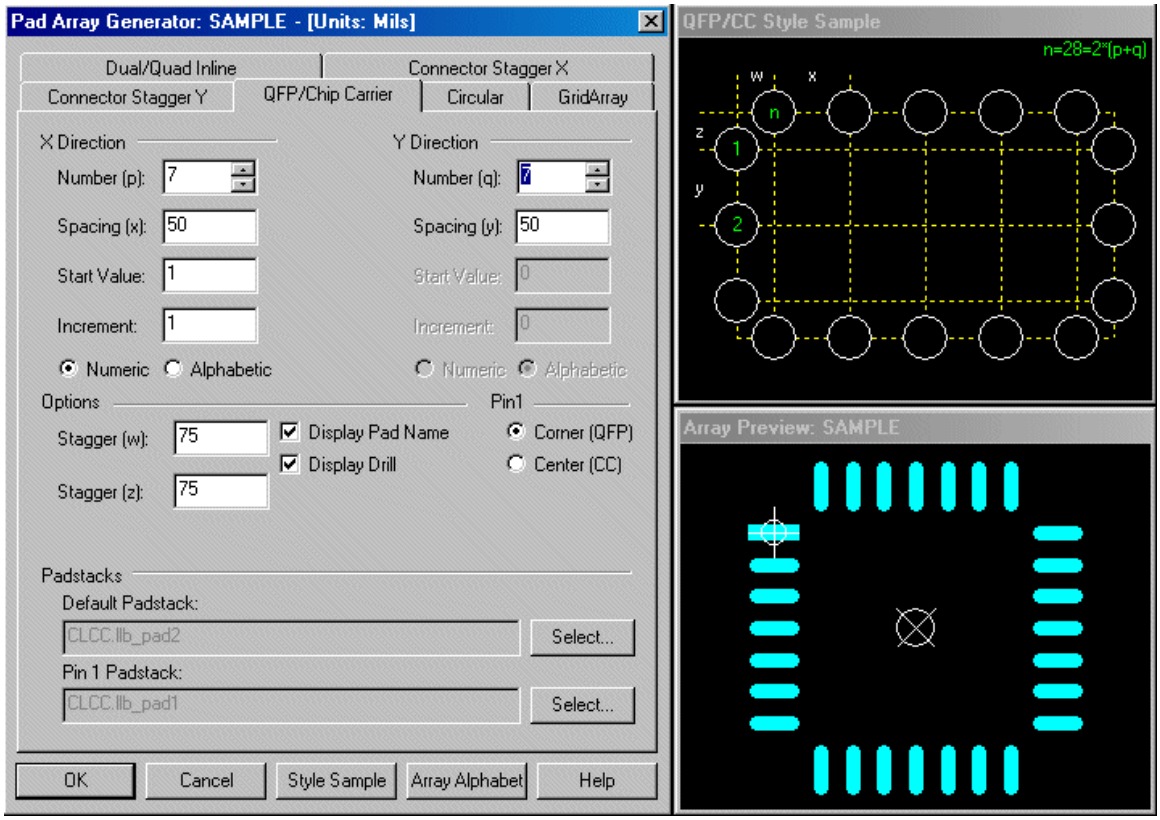

FIGURE 15: The Pad Array generator dialog box and preview window

3. Choose the style of pad array to create by selecting the appropriate tab. There are six different styles to choose

   - Dual/Quad line – creates an array that is limited to two columns in the X direction
   - Connector Stagger X – creates an array that is numbered from left to right and top to bottom
   - Connector Stagger Y – creates an array that is numbered from top to bottom and left to right
   - QFP/ Chip Carrier – create a Quad Flat Pack or Chip Carrier array
   - Circular – create an array of pads in a circle
   - Grid Array – create a Grid array or a ball grid array

4. In the Padstacks area, press the Select button to select the default padstack. The select padstack dialog box opens (see Figure 16)

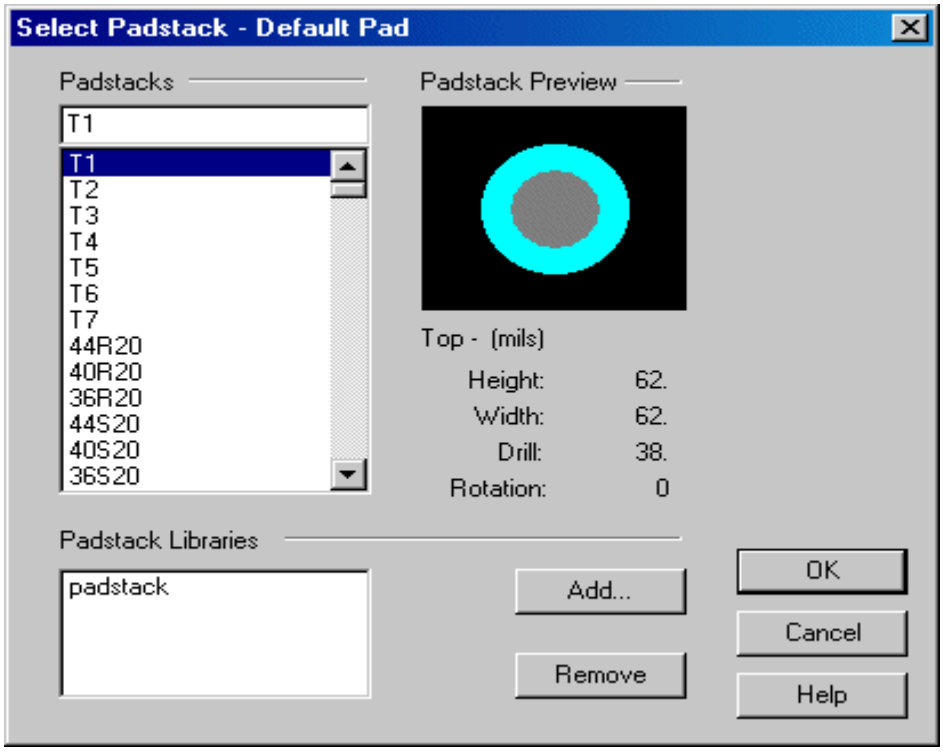

FIGURE 16: Select Pad stack Dialog Box

5. Select an appropriate padstack in the Padstacks area and click OK
6. If one needs a different padstack for pin1, press select to open the select padstack dialog box and choose the appropriate dialog box
7. Obtain spacing, stagger and other pad placement information from the part manufacturer's datasheet. Enter this data into X Direction, Y Direction and Options areas.
8. Click OK to generate the pad array

PARTS	PACKAGES
ATmega 128L	64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch0.50 mm, 5.40 mm Exposed Pad, Micro Lead Frame Package (MLF)
CC2420	QLP-48 package, 7x7 mm
DS2740	8-pin uMAX package
MAX3243	24-Pin SOIC Package

TABLE 4: Parts used in the Layout and their Packages

The footprints for ATmega 128L, CC2420, MAX3243, and DS2740 were created using the Pad array generator according to the packages described in Table 4. The footprints for all these components were stored in a custom made library called LAY.llb. Even the crystals footprint was slightly edited according to the datasheet for the crystal. After all the components were placed on the board and the appropriate footprints assigned to each component the board was ready for routing. The Figure 17 shows the board before routing.

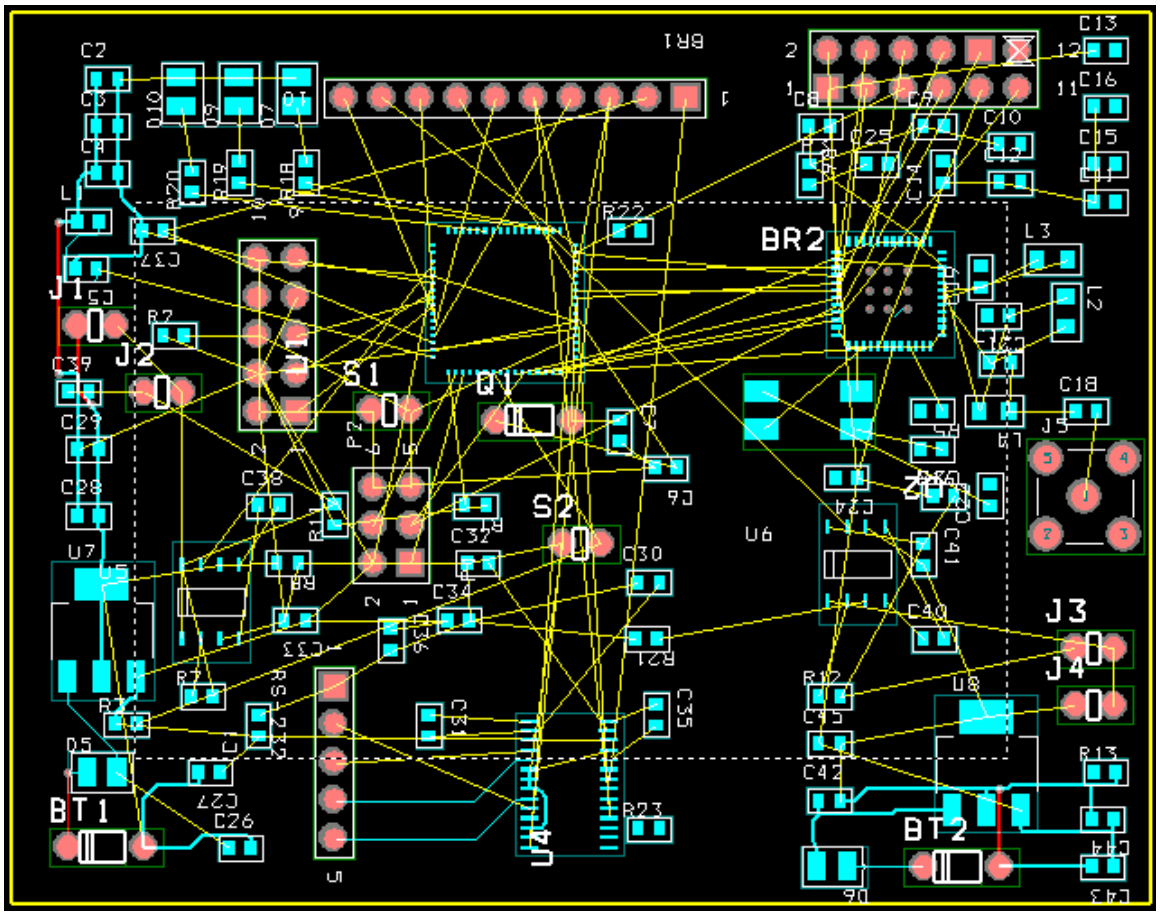

FIGURE 17: 802.15.4 board before routing

6.3 Routing the Board and Pouring Ground Planes for RF Section

The critical signals on the board such as the SPI interface between the ATmega 128L and CC2420 were routed manually. For proper RF shielding of the radio section, the ground of it was copper poured. The GNDB pin on the P3 header which is on the RF section of the board was used as the seed point for the copper pour. To designate a seed point

1. Choose the pin toolbar button.
2. Select a pin that is attached to the net to which you want to attach the copper pour zone.

3. From the pop-up menu, choose Toggle Copper Pour Seed. Layout marks the pin with an "X," to indicate that the pin is the copper pour seed point from which the copper will pour.

To create a copper pour the obstacle toolbar button was used. Right click on the design gives a pop-up menu from which New was selected. Then by clicking the left mouse button the RF section of the board was selected to be a copper pour. Then by using the CTRL key and left mouse button the new obstacle was selected. In its properties the obstacle type was selected as copper pour and the obstacle layer was selected as TOP. In the Net- Attachment drop down box the GNDB was selected as the net. Figure 18 shows the copper pour for the RF section. Some special considerations had to be taken regarding the width and height of the copper pour. These dimensions should not be multiples of the wavelengths of the radio frequency used for transmission and reception otherwise they will act as an antenna and create unwanted interferences.

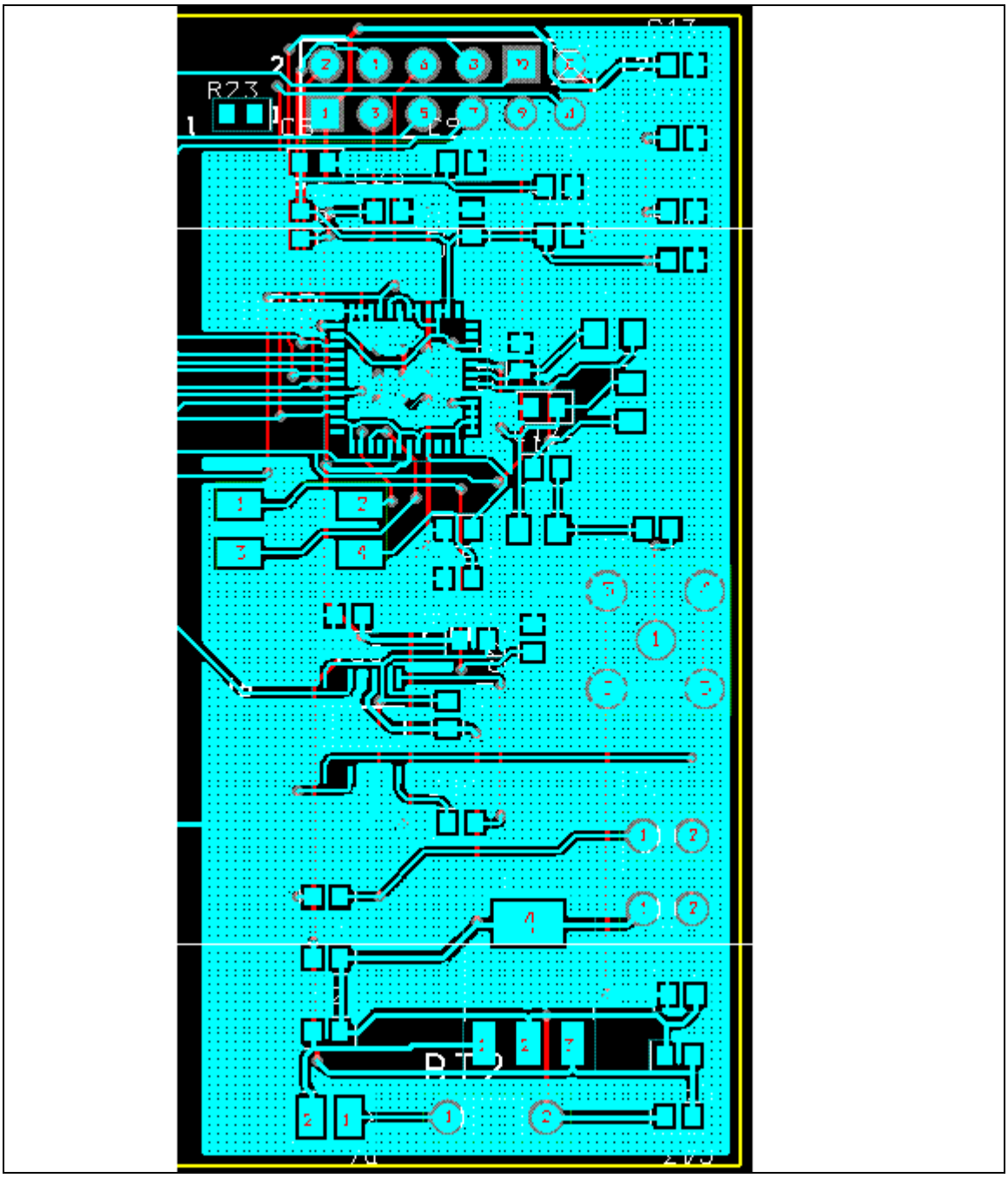

FIGURE 18: Copper Pour for the RF section

In the same manner as described above copper was poured surrounding the ATmega 128L section of the board. This pour provides a shield to the microcontroller from all the unnecessary electromagnetic waves in the surrounding. Another copper pour was made

on the bottom layer between the ATmega 128L and the header to shield the microcontroller section from electromagnetic interferences. The output from the CC2420 to the SMA connector was also routed manually to keep the output line short. After all the critical signals were routed manually the remaining portion was routed automatically using the Auto Route option in Layout. After the routing was complete the integrity of the design was verified using the Design Rules Check option in the Auto menu. Layout shows all the areas that have violated the design rules and are to be fixed. The Design Rules Check looks for the following errors in the design

- Placement spacing violations
- Route spacing violations
- Net rule violations
- Copper continuity violations
- Via location violations
- Off – grid vias
- Pad exit violations
- Test point violations
- Check copper pour

After completing the design rules check and fixing all the errors the design was cleaned up using the Cleanup Design option in the Auto menu. It eliminates the acute angles in the routing, optimizes vertices, shared tracks, shared Vias and pad exits. It also eliminates the unused nets, padstacks and footprints from the database.

6.4 Layers

6.4.1 Top Layer

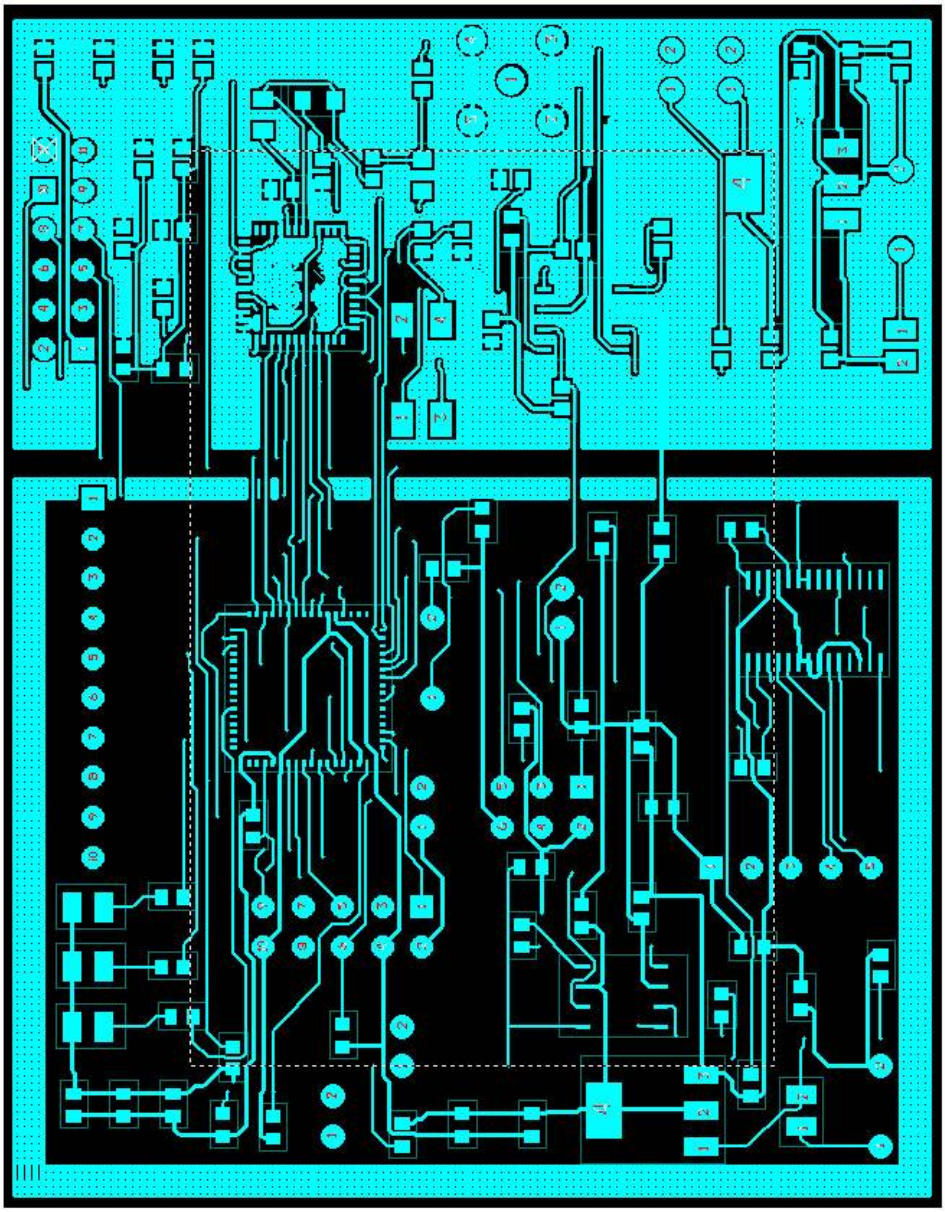

FIGURE 19: Routed TOP Layer of the Board

6.4.2 Bottom Layer

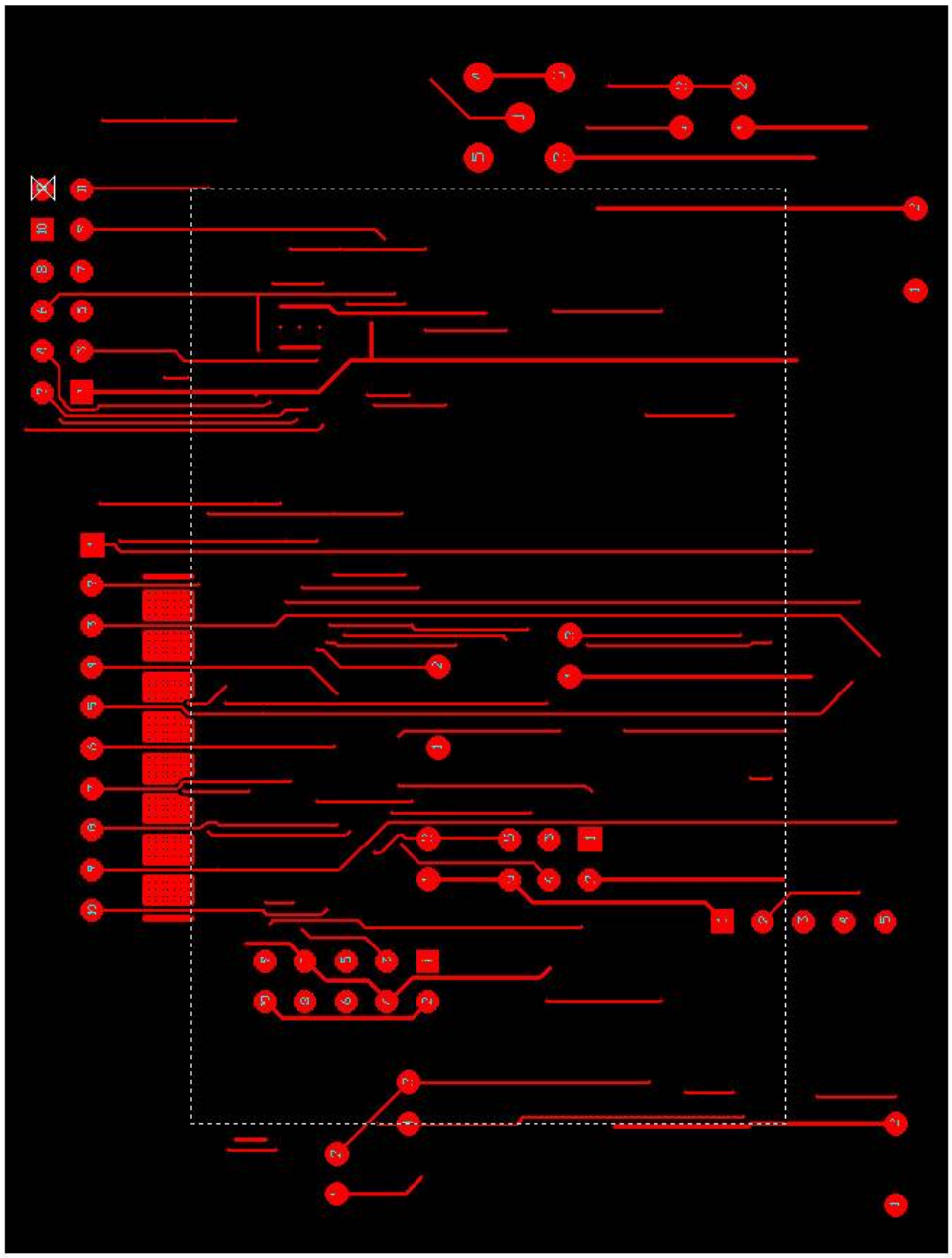

FIGURE 20: Routed Bottom layer of the Board

6.4.3 Final PCB Layout

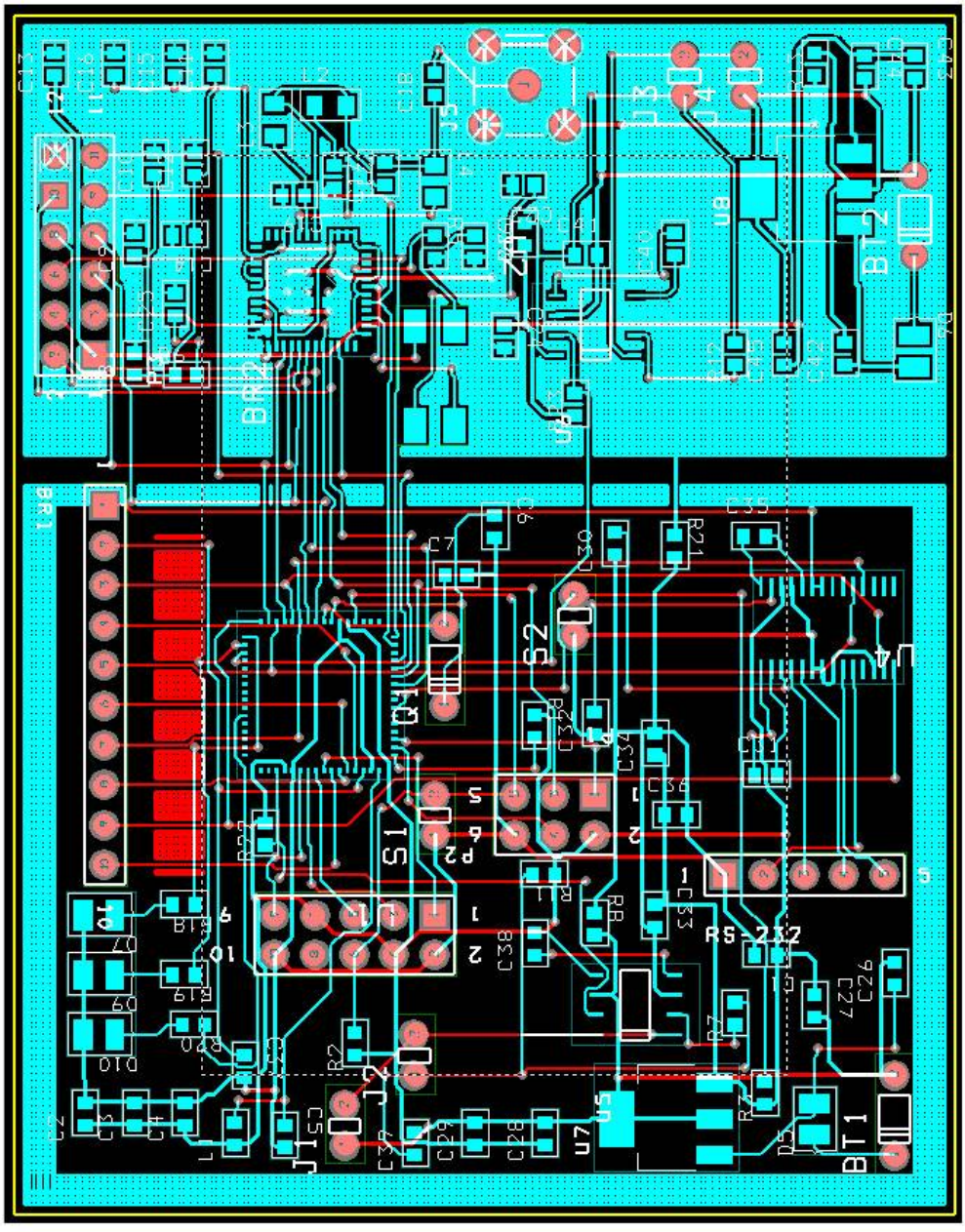

FIGURE 21: Final PCB Layout with both the Layers

6.5 Post Processing of the PCB Layout

After the layout of the board is complete the output files were to be generated for the manufacturing of the PCB. In Layout all the post processing functions are performed using the settings in the post process spreadsheet. The post process spreadsheet is displayed by clicking Post Process Settings in the options menu. The tile option in the windows menu was used to see both the post process spreadsheet and the design window. The Top and Bottom layers where verified by right clicking on the layer in the plot output file name column and selecting preview. This was done just to verify the design again. In addition to Gerber and Extended Gerber output, Layout offers DXF output for AutoCAD compatibility and HPGL output for printers and plotters. The layer output settings was specified in the post process spreadsheet by selecting a layer and clicking properties from the pop-up menu then editing the options in the post process settings dialog box which is shown in Figure 22.

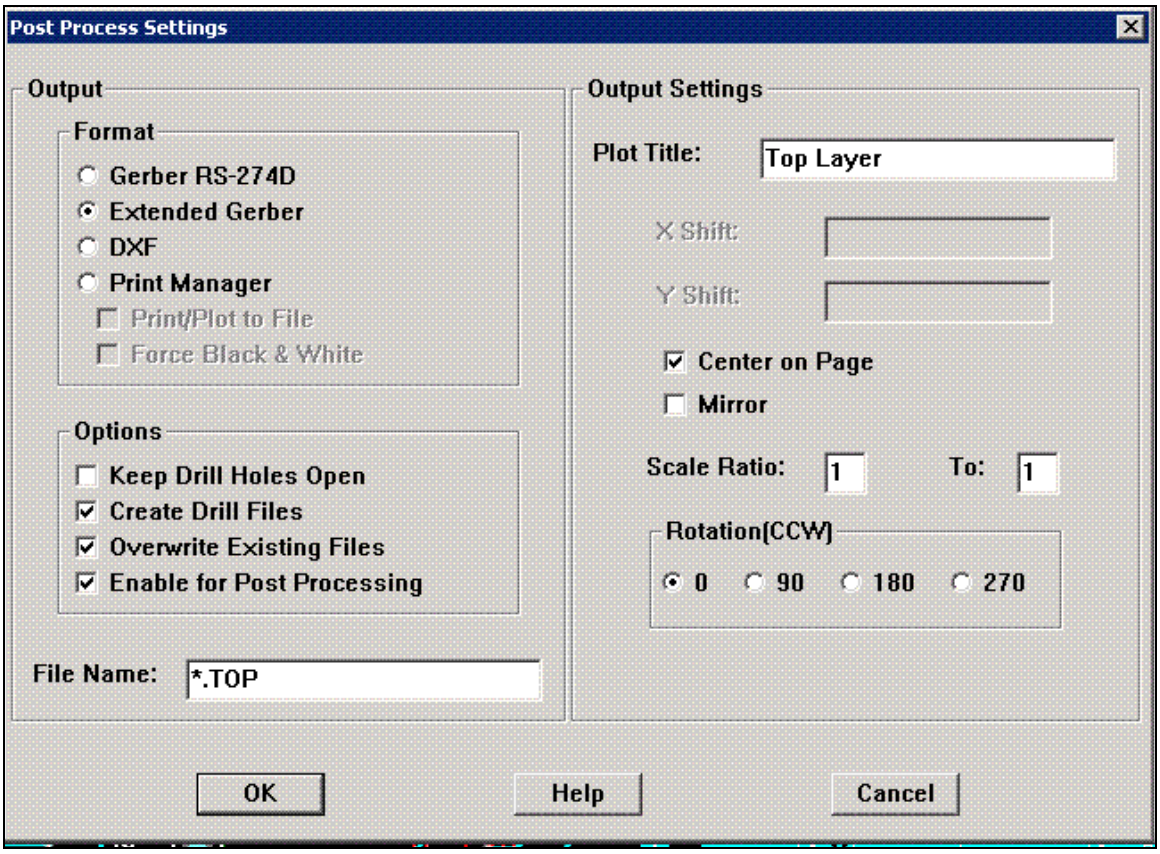

FIGURE 22: Post Process Settings Dialog Box

The process is done for both layers, Top and Bottom. Both the Gerber and Extended Gerber output files were created for the PCB because the Gerber format is used for photo plotter control. The photo plotter is used to create films used for etching. When the Gerber data is transferred from the customer to the template manufacturer; frequently the manufacturer does not receive information required for production such as the aperture list. In this case, it is necessary to confer with the customer regarding the missing information often leading to unnecessary telephone calls and a delay in production. For this reason, the Gerber format has been extended. This extended format is called "Extended Gerber" or "RS247X". The advantage of this format is that all necessary information for reading the Gerber file correctly is already contained in the file itself.

This means that no separate aperture list is required, because the definition of the aperture is already contained in the Extended Gerber file. The Top and Bottom layers had YES in the Batch Enabled column. These layers were processed by clicking run batch from the pop-up menu. To produce a drill tape, the create drill files option was checked in the post process settings dialog box, then by clicking run post processor from the Auto menu. Layout created a file named THRUHOLE.TAP.

CHAPTER 7: CONCLUSION

The main objective of this thesis was to create a low cost development and evaluation platform for testing the IEEE 802.15.4 with the main focus on power consumption measurement capability of the ATmega 128L microcontroller and the CC2420 RF Transceiver. The design flow of the evaluation board involved: specification definition, schematic design and PCB (Print Circuit Board) design.

The initial goal of this embedded board was to provide as an evaluation kit to analyze the communication between two wireless boards compliant with 802.15.4 and to measure the power consumed by the microcontroller and the CC2420 during transmit and receive modes. In addition to the hardware design, development support should be provided. This support should consist of software drivers, reference examples and proper documentation [15].

Testability was also taken into consideration while designing the board. The next step in the design flow is to build a prototype in order to verify the hardware design correctness. In order to do that a testing methodology has to be developed and the test results have to be analyzed [11]. The analysis of the test results will be used to redesign possible flaws in the design. To increase the flexibility of the evaluation platform, additional daughter boards should be developed to allow additional features, e.g., Bluetooth, USB and Wireless LAN communications. The 802.15.4 boards can be used in the future for developing a mesh network. The Mesh Network can be used in Automatic Meter Reading Systems and many other projects that require low power RF transceivers.

The evaluation board can also be developed with sensors and used for pollution monitoring, home automation and various other applications.

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APPENDIX A: DRILL LIST REPORT

****
DRILL LIST REPORT
U:\PC\WIN_DATA\DESKTOP\THESES-16.MAX
Fri Oct 28 17:43:03 2005
****

COMMENTS	DRILL	TOOL	XCOORD	YCOORD
		THRUHOLES		
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	10.00 m	1	-9066.67 m	6375.00 m
	10.00 m	1	-9066.67 m	6491.67 m
	10.00 m	1	-9041.67 m	6400.00 m
	10.00 m	1	-9041.67 m	6475.00 m
	10.00 m	1	-9008.33 m	5541.67 m
	10.00 m	1	-9000.00 m	5783.33 m
	10.00 m	1	-9000.00 m	6125.00 m
	10.00 m	1	-8983.33 m	5225.00 m
	10.00 m	1	-8933.33 m	4850.00 m
	10.00 m	1	-8933.33 m	5041.67 m
	10.00 m	1	-8925.00 m	5250.00 m
	10.00 m	1	-8925.00 m	5366.67 m
	10.00 m	1	-8900.00 m	5458.33 m
	10.00 m	1	-8700.00 m	5425.00 m
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APPENDIX B: COMPONENT LIST

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*
*
* Component List (Generic) *
*
*
* U:\PC\WIN_DATA\DESKTOP\THESES-16.MAX *
* Fri Oct 28 18:01:05 2005 *
*
*
****

REF DES	VALUE	PACKAGE	FOOTPRINT	X LOC	Y LOC	ROTATION
BR1	MSV10X2	MSV5X2	BLKCON.100/VH/TM1SQ/W.100/10	-7575.0..	6825	m 180
BR2	MSV4	MSV4	CRYSTAL	-7375.0..	6050	m 0
BT1	BATTERY	BATTERY	JUMPER200	-9200	4850	m 0
BT2	BATTERY	BATTERY	JUMPER200	-6950.0..	4800	m 0
C1	100nF	C	SM/C_0603	-8700.0..	5144	m 90
C2	100nF	C	SM/C_0603	-9125.0.	6875	m 0
C3	100nF	C	SM/C_0603	-9125.0.	6750	m 0
C4	100nF	C	SM/C_0603	-9125.0.	6625	m 0
C5	100nF	C	SM/C_0603	-9125.0.	6375	m 180
C6	22pF	C	SM/C_0603	-7600	5850	m 180
C7	22pF	C	SM/C_0603	-7750	5975	m 270
C8	100nF	C	SM/C_0603	-7250	6750	m 0
C9	10nF	C	SM/C_0603	-6950	6750	m 0
C10	68pF	C	SM/C_0603	-6750	6700	m 0
C11	68pF	C	SM/C_0603	-6500	6550	m 0
C12	68pF	C	SM/C_0603	-6750	6600	m 0
C13	100nF	C	SM/C_0603	-6500	6950	m 0
C14	100nF	C	SM/C_0603	-6900	6600	m 90
C15	100nF	C	SM/C_0603	-6500	6650	m 0
C16	68pF	C	SM/C_0603	-6500	6800	m 0
C17	C	C	SM/C_0603	-6775	6125	m 0
C18	5.6pF	C	SM/C_0603	-6550	6000	m 0
C19	5.6pF	C	SM/C_0603	-6800	6325	m 90
C21	0.5pF	C	SM/C_0603	-6725	6250	m 180
C22	27pF	C	SM/C_0603	-6775	5750	m 90
C23	27pF	C	SM/C_0603	-6900	5900	m 180

C24	10uF	C	SM/C_0603	-7125	5825	m 180
C25	10uF	C	SM/C_0603	-7100	6650	m 0
C26	2.2uF	C	SM/C_0603	-8775	4850	m 0
C27	2.2uF	C	SM/C_0603	-8800	5050	m 180
C28	33nF	C	SM/C_0603	-9175	5725	m 0
C29	100uF	C	SM/C_0603	-9175	5900	m 0
C30	100nF	C	SM/C_0603	-7700	5550	m 0
C31	100nF	C	SM/C_0603	-8250	5200	m 270
C32	100nF	C	SM/C_0603	-8150	5600	m 0
C33	33nF	C	SM/C_0603	-8575	5450	m 180
C34	470uF	C	SM/C_0603	-8200	5450	m 0
C35	100nF	C	SM/C_0603	-7653	5228	m 270
C36	2.2uF	C	SM/C_0603	-8350	5425	m 270
C37	100nF	C	SM/C_0603	-8950	6475	m 180
C38	100nF	C	SM/C_0603	-8700	5750	m 0
C39	100nF	C	SM/C_0603	-9200	6050	m 0
C40	C	C	SM/C_0603	-6950	5400	m 0
C41	100nF	C	SM/C_0603	-6950	5650	m 270
C42	2.2uF	C	SM/C_0603	-7225	4975	m 0

APPENDIX C: BILL OF MATERIALS

802.15.4 Board.

Bill Of Materials

Item	Quantity	Reference	Part	Size
1	1	BR1	MSV5X2	BLKCON.100/VH/TM1SQ/W.100/10
2	2	BT1,BT2	BATTERY	Jumper200
3	18	C1,C2,C3,C4,C5,C8,C13, C14,C15,C30,C31, C32,C35, C37,C38,C39,C41, C40	100nF	603
4	2	C6,C7	22pF	603
5	1	C9	10nF	603
6	4	C10,C11,C12,C16	68pF	603
7	2	C18,C19	5.6pF	603
8	2	C21,C17	0.5pF	603
9	2	C22,C23	27pF	603
10	2	C24,C25	10uF	603
11	5	C26,C27,C36,C42, C43	2.2uF	603
12	3	C28,C33,C44	33nF	603
13	2	C29,C45	100uF	603
14	1	C34	470uF	603
15	2	D5,D6	DIODE	805
16	3	D7,D9,D10	LED	805
17	4	J1,J2,J3,J4	JUMPER	
	1	J5	CON5	
18	1	L1	BLM11A102S	603
19	2	L2,L4	7.5nH	805
20	1	L3	5.6nH	805
21	1	P1	ISP	
22	1	P2	JTAG CONN	
23	1	P3	MSV12	
24	1	P6	BNC	
25	1	Q1	X_8.0/20/30/10/16	CRYSTAL
26	1	RS-232	MSV5	

27	3	R1,R2,R3	47K	603
28	1	R5	43K	603
29	1	R6	2 ohms	603
30	2	R7,R12	1k	603
31	2	R8,R13	0.02	603
32	2	R11,R16	150	603
33	3	R18,R19,R20	270	603
34	1	R21	0	603
	2	R22,R23	4.7K	603
35	2	S1,S2	PUSH_BUTTON	Jumper100
36	1	U1	ATmega128L	
37	1	U2	CC2420	
38	1	U4	MAX3243	
39	2	U5,U6	DS2740	
40	2	U7,U8	MIC5209-3.3BS	
41	1	X_16.00/10/10/10/16	CRYSTAL	