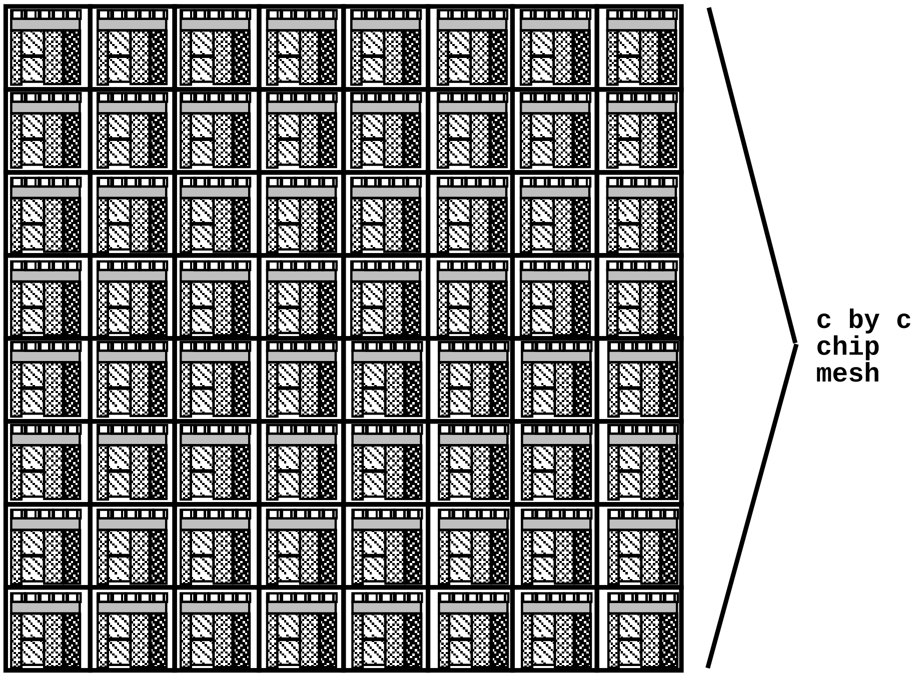
c by c
chip
mesh

Figure 8.2: Example of Chip Layer of our Multi-chip Module Package

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Definition 8.2 *The* chip layer *is made of a mesh of rows and columns of chips. The arrangement of chips in the mesh is determined prior to assignment of the chip interconnections. The chips are assigned to form a* $c \times c$ *mesh. No communications interconnections are allowed on the chip level. Not all locations in the chip layer need to be occupied. Figure 8.2 shows the chip layer of our MCM package.*

Definition 8.3 *The* links *are the components of chip to chip interconnections. Links are a single path in the X- or Y-direction of a layer. Connections between two layers are* vias.

Definition 8.4 *The* communications tracks, *or simply* tracks, *of an interconnection layer are the possible straight physical paths that a link can use. Each interconnection*